mi

TF 2414A

COUNTER/TIMER

INSTRUCTION MANUAL

MARCONI INSTRUMENTS LIMITED

Alternative Colour Coding
for Mains Leads
(Red - Black - Green series)

WARNING

The colour coding on mains leads is being changed to conform with international recommendations. During the change-over period, the instrument with which this manual is issued may be wired in either the old or new colours as follows:

	Old colour code	New colour code	Sleeve symbol
LINE (PHASE)	Red	Brown	
NEUTRAL	Black	Blue	N
EARTH (GROUND)	Green	Green/Yellow	⏚

EBA - 3
1 - 5/69

Youtube.com/TonyAlbus
73 Tony PE1ONS

INGENIEURSBUREAU
KONING en HARTMAN N.V.
TELEFOON (070) 678380* TELEX 31528

55142 ONTWIKKELING PRODUKTGROEP 20

Instruction Manual

No. EB 2414A

for

COUNTER/TIMER

TF 2414A

AA.001830.

CHANGE OF FREQUENCY UNIT

Marconi Instruments, in accordance with international usage, has decided to adopt the hertz (Hz) as the name of the unit of frequency in place of the cycle per second (c/s). During the transition period the frequency units in this instruction manual may not agree with those on the equipment. The value of the alternative units and that of their multiples – kHz and kc/s, MHz and Mc/s, GHz and Gc/s – is, however, identical.

© 1969

FEB. 1972

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND

..I. 2c
22/69

Contents

	Page
Chapter 1 GENERAL INFORMATION	5
1.1. Introduction	5
1.2. Data Summary	5
1.2.1. Power Supply	5
1.2.2. Frequency Measurement	5
1.2.3. Period Measurement	6
1.2.4. Timing	6
1.2.5. Count	7
1.2.6. Start and Stop Inputs	7
1.2.7. External Reference Input	7
1.2.8. Test Frequency Output	7
1.2.9. Standard Frequency Output	7
1.2.10. Data Logging Output	8
1.2.11. Display	8
1.2.12. Weight and Dimensions	8
1.3. Accessories	8
1.4. Accuracy of Electronic Counters	8
Chapter 2 OPERATION	10
2.1. Mains-Voltage Setting	10
2.2. Supply Connection	10
2.3. Test Facility	10
2.4. Frequency Measurement	11
2.4.1. Principle of Operation	11
2.4.2. Measurement Procedure	12
2.5. Multi-Period Measurement	13
2.5.1. Principle of Operation	13
2.5.2. Measurement Procedure	14
2.6. Timing	14
2.6.1. Principle of Operation	14
2.6.2. Timing A-A Measurement Procedure	15
2.6.3. Timing B-C Measurement Procedure	15
2.7. Count	16
2.7.1. Principle of Operation	16
2.7.2. Measurement Procedure	16
2.8. Standard Frequency Output	16
2.9. External Reference Facility	17
2.9.1. Frequency Ratio Measurement	17
2.10 Data Logging Output Facility	19
Chapter 3 MAINTENANCE	20
3.1. Case Removal	20
3.2. Fuse Replacement	20
3.3. Checking and Adjustment of d.c. supplies	20
3.4. Checking and Adjustment of Oscillator Frequency	21
3.5. Digital Indicator and Printed Circuit Board Replacement	21
3.6. Decimal Point Lamp Replacement	21
3.7. Maintenance of Pulse Shaper Board	22
3.8. Colour Coding of Leads	22
Chapter 4 BASIC SYSTEM—DESCRIPTION OF CIRCUITRY	24
4.1. Circuit Diagrams and Plug-in Board Complement	24
4.2. General Circuit Description	24
4.2.1. Mains and Internal Supplies	24
4.2.2. Input (A) Signal Circuit	25

	Page
4.2.3. Reference Signal Circuit	25
4.2.4. Frequency Divider Chain and Standard Frequency Output	25
4.2.5. Gate and Control Circuits	26
4.2.6. Counter Chain and Display	26
4.2.7. Display Time and Reset Circuit	27
Chapter 5 DETAILED CIRCUIT DESCRIPTION OF SUB-UNITS	28
5..1. Pre-Amplifier, type 66/004	28
5..2. Positive/Negative Polarity Selector, type 66/006	28
5..3. Double Decade, type 66/100	28
5..4. Decade Divider, type 66/140	29
5..5. Power Supply, type 66/210	30
5..6. Pulse Shaper, type 66/330	31
5..7. Oscillator, type 66/520	31
5..8. Gate Control and Reset Circuit, type 66/630	32
5..9. Low Speed Counter and Memory, type 66/710M	34
5..10 High Speed Counter and Memory, type 66/730	34
5..11 High Speed Integrated Counter and Memory, type 66/740M	35
Chapter 6 REPLACEABLE PARTS	36
6..1. Ordering Information	36
6..2. Pre-amplifier, type 66/004 (diagram E67/63)	36
6..3. Positive/Negative Polarity Selector, type 66/006 (diagram E67/80)	37
6..4. Double Decade, type 66/100 (diagram ES66/29)	37
6..5. Decade Divider, type 66/140 (diagram ES66/36)	37
6..6. Power Supply, type 66/210 (diagram E66/98)	38
6..7. Pulse Shaper, type 66/330 (diagram E67/83)	39
6..8. Oscillator, type 66/520 (diagram E67/82)	39
6..9. Gate Control and Reset Circuit, type 66/630 (diagram E67/60)	40
6..10 Low Speed Counter and Memory, type 66/710M (diagram ES66/89)	42
6..11 High Speed Counter and Memory, type 66/730 (diagram ES66/90)	42
6..12 High Speed Integrated Counter and Memory, type 66/740M (diagram E67/85)	43
6..13 Components on Main Chassis (diagram E67/81)	43

ILLUSTRATIONS

	Circuit or General Drawing No.
General Layout of Counter Type TF 2414A	S66/90
Counter Type TF 2414A, Main Circuit Diagram	E67/81
Pre-amplifier, type 66/004	E67/63
Positive/Negative Polarity Selector, type 66/006	E67/80
Double Decade, type 66/100	ES66/29
Decade Divider, type 66/140	ES66/36
Power Supply, type 66/210	E66/98
Pulse Shaper, type 66/330	E67/83
Oscillator, type 66/520	E67/82
Gate Control and Reset Circuit, type 66/630	E67/60
Low Speed Integrated Counter and Memory, type 66/710M	ES66/89
High Speed Integrated Counter and Memory, type 66/730	ES66/90
High Speed Integrated Counter and Memory, type 66/740M	E67/85

Chapter 1

General information

1.1. INTRODUCTION

This instrument is a versatile counter for the measurement of Frequency and Frequency-ratio, Period measurement (by single period or multi-period sampling), Timing and for general purpose Counting.

The readout is presented by six side-view neon indicator tubes which are mounted behind a display screen for optimum contrast. A display Memory facility enables a reading to be retained while another is being made.

The accuracy of all time-dependent measurements is determined by the reference source which is an oven-controlled 2 MHz high stability quartz crystal oscillator. A 2 MHz Test frequency output and a Standard Frequency output (selectable in decade steps from 0.1 Hz to 1 MHz) are obtainable at front-panel-mounted sockets. Sensitivity and display time controls are incorporated and provision is made for the gating circuit to be controlled by external signals and for the use of an external reference source.

A Data Logging Output for printer drive, etc., is an optional feature which is provided only if initially ordered. This version is identified by the type number, TF 2414A/1.

Silicon semi-conductor devices are used throughout the equipment which consists essentially of plug-in printed circuit boards. The outer housing of the unit comprises a ventilated p.v.c. covered dual-sectioned wrap; this may be easily removed to give access to the interior of the instrument. A swivelling carrying handle of aluminium alloy is fitted and may be locked in position to form a tilt stand.

1.2. DATA SUMMARY

1.2.1. Power Supply

100-125 V, 40-60 Hz or 400 Hz
or, 200-250 V, 40-60 Hz or 400 Hz
(for voltage adjustment see Section 2.1)
Consumption: approximately 35W.

1.2.2. Frequency Measurement

Frequency Range:	10 Hz to 40 MHz	
Accuracy:	± 1 count ± crystal stability Crystal frequency: 2 MHz Crystal stability: ± 1 part in 10^6	
Signal Specification:		
Minimum Amplitude,	(Sine-wave input) 10 mV r.m.s., 10 Hz to 20 MHz 20 mV r.m.s., above 20 MHz (Pulse input) 30 mV, peak	
Maximum Amplitude,	(Sine-wave input) (Pulse input)	250 V 400 V
Maximum D.C. level of input		400 V

Pulse Response: The instrument is triggered by negative-going pulse edges only.
Paired pulse resolution: (typically) 25n pulses, spaced at 25ns apart.

Input Impedance (Min.): 1 MΩ ± 10% shunted by 10 pF

Gating Times (selectable): 1 µs to 10 sec. in decade steps

Count Capacity: 999999

1.2.3. Period Measurement

Range: 10 Hz to 1 MHz

Accuracy: As for Frequency measurement ± Trigger level error

Trigger level error -

With input signals of low frequency and near-minimum amplitude the error on the ranges is -

Range	:	Error
1	:	±0.3%
10	:	±0.03%
10^2	:	±0.003%

The error is reduced by a factor of ten for each subsequent range

The accuracy on each range improves rapidly with increase in signal amplitu above 10 mV r.m.s.

Signal Specification: As for Frequency Measurement

Input Impedance: As for Frequency Measurement

Count Capacity: As for Frequency Measurement

Gating Times: On Multi-Period: 1 to 10^7 periods, selectable in decade steps
On Timing A-A: 1 period of input waveform

Timing Units: On 'Multi-period': 1 µs

On 'Timing A-A': 1 µs to 10 s selectab in decade steps

1.2.4. Timing

Range: 1 µs to 9999990 seconds

Count Capacity: As for Frequency measurement

Accuracy: ± 1 µs $^{+0}_{-1}$ timing unit

Timing Units: 1 µs to 10 s in decade steps

For gate control Start and Stop signals see Section 1.2.6.

1.2.5. Count

Count Capacity	As for Frequency measurement
Frequency Range:	As for Frequency measurement
Signal Specification:	As for Frequency measurement
Input Impedance:	As for Frequency measurement

For gate control Start and Stop signals see Section 1.2.6.

1.2.6. Start and Stop Inputs

For external gate control on functions TIMING B-C and COUNT

Triggering:	Each gating action (i.e., Start and Stop) can be triggered by a pulse input, contact closure, or by manual switching.
Pulse Input:	For each input line, (a.c. coupled), positive or negative going pulses, selectable. Minimum amplitude: 4V for a maximum rise time of 1 µs Maximum amplitude: 50V for a maximum rise time of 12.5 µs
Input Impedance: (each line)	Up to 6V: approx. 50kΩ in parallel with 150 pF Above 6V: approx. 100kΩ in parallel with 5,000 pF

Alternative control by momentary short-circuit of the appropriate (Start and Stop) input socket to chassis-earth, or by momentary depression of the appropriate (Start or Stop) push button.

1.2.7. External Reference Input

Frequency:	100 Hz to 1.5 MHz (Refer to Section 2.9)
Signal Amplitude:	0.5 V to 50 V r.m.s.
Input Impedance:	50 kΩ in parallel with 100 pF

1.2.8. Test Frequency Output

Frequency:	As selected Reference Frequency (2 MHz when Internal Reference is selected)
Signal Amplitude:	greater than 2.5 V peak to peak
Waveform:	Sinusoidal
Output Impedance:	1.5 kΩ

1.2.9. Standard Frequency Output

Frequency:
(Determined by the setting of the Range switch when the Function Selector is set to FREQUENCY)
(For signals produced at this output when the Function Selector setting is other than FREQUENCY, see Section 2.8)

(i) With the Internal Reference selected - 1 MHz to 0.1 Hz selectable in decade steps.

(ii) With External Reference selected - External reference frequency divided by 1 to 10^6, selectable in decade steps.

Signal Amplitude: Approx. 5 V peak to peak

Waveform:	Rectangular
Output Impedance:	Approx. 5 kΩ

TF 2414A/2 and A/3 has 1 MHz Standard Output suitable for use with Frequency Converter, TF 2400 Series.

1.2.10. Data Logging Output

Applicable only to counters bearing the type number, TF 2414A/1 and A/3

	4 lines per digit, plus print command line Code: 1-2-4-8 b.c.d.
Digit Lines:	'1': More positive than + 3.5 V '0': Between 0 V and + 0.5 V (Open-circuit d.c. levels with respect to chassis-earth) Output Impedance approx. 1 kΩ
Print Command Signal:	5 V negative-going pulse: Rise-time approx.: 200 ns Pulse width approx.: 40 µs Output Impedance: Not greater than 1 kΩ

1.2.11. Display

On the AUTOMATIC setting, the Display Time is adjustable between approximately 0.5 and 5 seconds: on the 'Infinity' setting, the display is retained until the Reset push-button is depressed.

Memory switch set to:

'OFF'	Memory facility unused: the display time is as above.
'ON'	Readout retained until the end of a new sampling period.

1.2.12. Weight and Dimensions

Weight (approx.)	Case dimensions (approx.) -		
	Width	Height	Depth (front to rear
12½ lb.	10-3/8 in.	5-1/8 in.	12-1/8 in.
(5.7 kg)	(26.4 cm.)	(13 cm)	(30.8 cm)

1.3. ACCESSORIES

1.3.1. Accessories Supplied

TF 2414A and A/2	3 - B.N.C. Free plugs
TF 2414A/1 and A/3	3 - B.N.C. Free plugs 1 - 36-way Free plug, Amphenol 57-30360

1.3.2. Optional Accessories

Rack Mounting kit, TM 9852

1.4. ACCURACY OF ELECTRONIC COUNTERS

In general there will always be a possible error of ± 1 count on the least significant digit. This, together with the discrimination required, will determine whether Frequency or Period measurement is used.

1.4.1. Frequency Measurement

Accuracy is determined by the stability of the internal standard which provides the accurate counting interval. In addition there will be the ± 1 count and thus for a given gate time higher frequencies will be displayed with the greatest discrimination and accuracy.

1.4.2. Period Measurement

The errors in period measurement will be -

(a) ambiguity of gate triggering level.
(b) Accuracy of internal timing units.
(c) The ± 1 count

For sine wave inputs the total possible error may be expressed as

$$\frac{1}{\sqrt{n}} \times \frac{En}{Es}$$ where

En = total noise, including that due to counter circuitry,
Es = signal level,

or $$\frac{1}{n\sqrt{n}} \cdot \frac{En}{Es}$$ where n is the number of periods in multi-period measurements

1.4.3. Phase Measurement

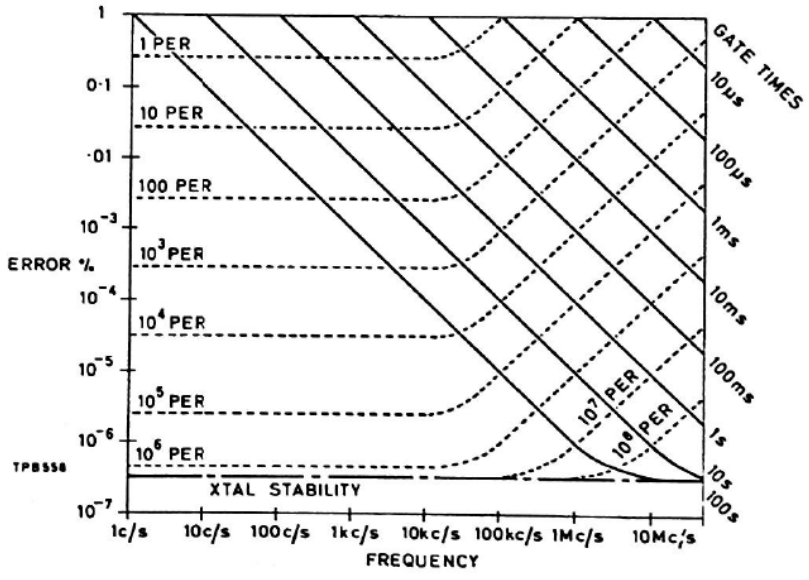
The reference and out of phase signals are used to start and stop the counter, the latter being arranged for period measurement and time interval measurement.

$$\phi = 360^{o} \frac{t}{T}$$ where

ϕ = phase difference in degrees,
t = phase difference in counter timing units,
T = period of signal in counter timing units.

Thus if the counter is to read directly in degrees external timing units must be provided of a frequency n.360 fs where n is an integer determining the discrimination desired and fs is the frequency of the signal to be measured. The accuracy obtained is a function of the ambiguity of the triggering level.

ACCURACY CHART



Chapter 2

Operation

2.1. MAINS-VOLTAGE SETTING

The mains transformer of the internal power unit has twin primary windings which may be series-connected for operation on supply voltages in the range 200 to 250 V a.c., or parallel-connected for operation on supplies in the range 100 to 125 V a.c.

The instrument is normally despatched set for 200 to 250 V a.c. operation.

To select the other voltage-range, first remove both sections of the case. To remove a section, withdraw the 4 BA fixing screw from either side, slide the cover backwards sufficiently to disengage the front edge from the panel surround; then lift away.

The plug-in power unit is situated adjacent to the rear panel: withdraw its three fixing screws (arranged in triangular formation around the cut-out on the underside of the chassis), disengage the flying-plug and remove the unit from the instrument.

The primary windings are terminated on that side of the transformer where the tags are arranged as shown below -

120 V - live input-line
0 V
120 V
0 V - neutral input-line
(the base of the power unit)

The 'live' and 'neutral' lines should remain connected as indicated above.

For 100 to 125 V a.c. connect the windings in parallel (i.e., link the 120 V tags together and link the 0 V tags together).

For 200 to 250 V a.c. connect the windings in series (i.e., link together by means of a soldered wire, the two inner tags).

Replace and secure the power unit, re-connect the flying-plug and secure the instrument case before connecting the supply.

2.2. SUPPLY CONNECTION

With the mains transformer appropriately connected (see Section 2.1) and with the POWER switch OFF, connect the three-core mains cable to the supply. The cores will conform to one of the two colour-codes given below -

Brown, or Red core	:	mains live
Blue, or Black core	:	mains neutral
Green and Yellow, or Green core	:	earth

2.3. TEST FACILITY

Although measurements may be taken immediately after the supply has been switched ON, in order that the degree of accuracy achieved shall conform to the specification, a period of at least 15 minutes should be allowed to elapse for temperature stabilization of the internal crystal oven. The oven is operative on all functions, but no warm-up period is necessary if the function to be used is Count,

for then the output of the crystal oscillator is unused and results are independent of oscillator frequency.

To check the counting and readout operations of the instrument set the rear-mounted Crystal Reference switch to 'INT', feed the output of the Test socket (2 MHz) to the coaxial A-Input socket (centre-pin) and set the Sensitivity control to 'MAX', i.e., fully clockwise.

To enable the progress of the count to be observed, the Memory switch should be set to 'OFF'.

Listed below for each setting of the 8-position Range switch are the displays which should be presented for the 'Frequency', 'Multi-period' and 'Timing A-A' positions of the Function Selector.

If the Display Time switch is set to 'INF', a new count may be initiated by momentary depression of the Reset push-button.

If the switch is set to 'AUTO', measurements will occur automatically, the duration of the display being dependent upon the setting of the Display Timer.

Range Switch	Function Selector Setting		
Setting	Frequency	Multi-period	Timing A-A
1	000002 ±1	000001 ±1	000001 ±1
10	00002.0±1	000005 ±1	0000.00 ±1
10^2	0002.00±1	000050 ±1	00000.0 ±1
10^3	002.000±1	000500 ±1	000000 ±1
10^4	02000.0±1	005000 ±1	0000.00 ±1
10^5	2000.00±1	050000 ±1	00000.0 ±1
10^6	000.000±1	500000 ±1	000000 ±1
10^7	00000.0±1	000000 ±1	000000 ±1

Results for the '10^7' setting are presented after a 10 second gating time.

Operation for the Function Selector setting 'Timing B-C' is perhaps most easily checked with the Range switch set to 10^4. Momentarily depress the Reset push-button. Upon a momentary depression of the Start toggle to the Manual position the instrument should commence to count; the display being presented in 'Seconds' (with the decimal point centrally positioned). The second most significant digit should increase at one count per second until timing is stopped by momentary depression of the Stop toggle.

All internal gating, counting and readout circuits will have been checked during the above operations; the following procedure will therefore suffice to check the Function Selector circuit for the setting 'Count A/B-C'. Set the Function Selector to 'Count A/B-C', then momentarily depress the Reset push-button. Upon momentary depression of the Start toggle, cycles of the 2MHz Test frequency (applied at input A) will be counted and therefore give rise to a rapid change in display which will cause all digits of each display tube to be illuminated simultaneously. However, upon momentary depression of the Stop toggle a distinct display should be presented.

2.4. FREQUENCY MEASUREMENT

2.4.1. Principle of Operation

In this function, the setting of the 8-position Range switch determines which of eight internal signal frequencies, derived

from the reference oscillator, shall control the gate; it thus determines the gating time.

During this time, cycles of the A-input frequency pass via the gate and are counted by a chain of decade/indicator-drive stages. The indicators then present the resultant count. Where appropriate a decimal point is included in the display so that the result is in MHz, kHz or Hz as indicated by the setting of the Range switch.

2.4.2. Measurement Procedure

(i) Set the rear-mounted Crystal Reference switch to 'INT' (If an external reference source is to be used, refer to Section 2.9).

(ii) If the data logging output facility (on TF 2414A/1) is to be used, refer to Section 2.10.

(iii) Set the Display Timer to either -

1. 'INFinity': for this setting the Reset push-button must be momentarily depressed for a measurement to be initiated or

2. 'AUTOmatic': for this setting measurements are initiated automatically; the duration of each readout is determined by the setting of the Display Timer (minimum setting approximately 0.3 second; maximum setting approximately 5 seconds).

Set the Memory switch as required,

OFF : For each measurement the indicators show the progression and result of each count.

ON : Only the result of the count is displayed; it is retained until the end of the next gating period whereupon the new count is shown.

On this setting, depression of the Reset push-button resets the counter circuit but the display remains unchanged.

With the Memory facility ON, no visible change will occur in the display should the new count be the same as the previous result.

When overflow occurs with the Memory switched OFF, the extreme left hand indicator can be seen to reset from 9 to 0, whereas with the Memory switched ON no such evidence of overflow is available since only the final result held by the counters is made visible. It is therefore advisable to determine initially the magnitude of a measurement with the Memory OFF.

(iv) Turn the Sensitivity control initially to 'MAX'.

This setting is suitable for smooth-edged waveforms of any amplitude within the acceptable range of the instrument. When interference is present, or the leading and/or trailing waveform-edges are irregular (e.g., due to harmonic distorti reduce the sensitivity setting. A few initial measurements will show if the instrument is triggered more than once in a cycle, as indicated by excessive counts. In general a sensitivity setting consistent with input amplitude is desirable. The control is most effective at low input frequencies owing to its low pass filter action.

(v) Connect the input signal lead to the coaxial socket 'A' (Centre-pin: 'high' signal line. Shell: Chassis earth).

(vi) Set the Function Selector to 'FREQUENCY' (marked in black on the panel). The corresponding black scale of the Range switch is applicable to displays on this function. Set the switch to a range suitable for measuring the input frequency. When the order of frequency is unknown first use the highest range (1 µs gating time).

The gating times for the switch positions (clockwise order) are as follows -

Range switch position		Gating Time
1	(MHz)	1 µs
2	"	10 "
3	"	100 "
4	"	1 ms
5	(kHz)	10 "
6	"	100 "
7	"	1 second
8	(Hz)	10 seconds

(vii) Momentarily depress the Reset push-button for a measurement to be initiated. (On the 'AUTO' setting, measurements will then subsequently occur automatically).

The number displayed (which includes a decimal point for all Range switch settings except '1') is the frequency of the input signal in MHz, kHz or Hz as indicated by the setting of the Range switch.

Whether the count capacity of the instrument is exceeded during a measurement will depend upon the input frequency and the range employed. The most significant digit indicator resets from 9 to 0 when ever the count capacity is exceeded.

Example of Measurement -

A frequency of 100023.4 Hz measured over a gating time of 10 ms would produce the display 00100.0 (kHz) subject to the accuracy stated in Section 2.2. The same frequency measured over a gating time of 10 seconds would cause the count capacity to be exceeded once during the measurement and would produce the display 00023.4. The most significant digit (M.S.D.), i.e., 1, would therefore not be shown: the figure presented by the right hand indicator would be the 7th M.S.D.

Thus, in general, once the first few M.S.D's of a measurement have been determined, the frequency may be resolved to a greater accuracy by the use of longer gate times.

2.5. MULTI-PERIOD MEASUREMENT

On this function, single-period measurement is catered for by position '1' of the Range switch, the count being recorded in 1 µs timing units. Single period measurements may also be taken on function 'Time A-A' where the timing units are selectable (refer to Section 2.6.2.).

2.5.1. Principle of Operation

In this function, signals applied at input-A control the gate which is held open for 'n' periods of the input waveform, where 'n' is the setting (e.g., 10^2) of the Range switch. During the

gating time, pulses derived from the reference oscillator and which occur at a rate of 1 per microsecond pass through the gate to the counter/display circuit. The result is a measurement of the time (in microseconds) for which the gate is held open and is a period or multi-period measurement (depending upon the Range switch setting) of the input waveform.

2.5.2. Measurement Procedure

Carry out procedures (i) to (v), inclusive, of Section 2.4.2; then proceed as follows -

Set the Function Selector to 'MULTI-PERIOD' (marked in blue on the panel). The correspondingly coloured scale of the Range switch is applicable to this function. Set the switch to the number of periods over which the measurement is to be made, (1 to 10^7 periods in decade steps being selectable). The range selected should be chosen to suit the order of the input frequency so that the count capacity will not be exceeded. Once the first few digits of a measurement have been determined, other ranges (over which the count capacity may be exceeded) can be used for the determination of lesser significant digits; therefore, in general the lowest range '1' should be used first, then higher ranges progressively.

Momentarily depress the Reset Push-button for a measurement to be initiated. (On the AUTO' setting, measurements will then subsequently occur automatically).

The count is registered in microsecond units.

Example of Measurement

Consider a frequency in the order of 100 kHz with a period of 10.234567 µs measured first on range '1', the resultant display being 000010(µs). If range 10^6 were then used the count capacity would be exceeded ten times during the measurement and the resultant display would be 234567µs. Since this is produced over 10^6 periods of the input waveform the count should be divided by 10^6 to obtain the value 0.234567 µs for one period. Including the first two digits '10' (determined on the first gate-time range) gives 10.234567 µs as the period of the input signal.

Trigger Level Error

Results are subject to trigger level error which is indicated in repeated measurements by jitter of the least significant digit/s. The error is more pronounced with input signals of low frequency and near minimum amplitude; for such signals the error is -

Range	:	Error
1	:	±0.3%
10	:	±0.03%
100	:	±0.003%

The error is reduced by a factor of ten for each subsequent range.

The accuracy on each range improves rapidly with increase in signal amplitude above 10mV r.m.s.

2.6. TIMING

2.6.1. Principle of Operation

For Timing, two functions are provided. On 'Timing A-A' the gate is opened by the first pulse received at the A-input and is closed by the second. During the gating time pulses derived from the

reference oscillator pass through the gate at the rate of 1 per microsecond and thence pass via a frequency divider chain to the counter/display circuit. The Range switch determines the division factor of the frequency divider chain and therefore the unit of time in which the result is displayed.

On 'Timing B-C' the gate is opened and closed by signals applied at the B and C input sockets respectively, or by depression of the START and STOP toggles. The function of the timing signal circuit, however, is as described for the previous case.

2.6.2. Timing A-A Measurement Procedure

Carry out procedures (i) to (v) inclusive, of Section 2.4.2., then proceed as follows.

(a) Set the Function Selector to 'TIMING A-A' (marked in red on the panel).

(b) The red scale of the Range switch is applicable to displays on this function. Set the switch for the timing units in which the interval is to be measured; timing units of 1 μs to 10 seconds are available in decade steps from the first switch-position (μs) to the last switch-position (sx10) respectively.

(c) Connect the input signal lead to coaxial socket A.

(d) Momentarily depress the Reset push button.

For a Display Time switch setting of 'AUTO', further operation of this push-button is not required in taking successive measurements since reset action prior to each new measurement is triggered automatically.

Where appropriate a decimal point is included in the resultant display so that, providing the count capacity is not exceeded, the complete time measurement is displayed in the units of time (μs, ms or seconds) indicated by the setting of the Range switch.

2.6.3. Timing B-C Measurement Procedure

(i) Carry out procedures (i) to (iii) inclusive, of Section 2.4.2.

(ii) Set the Function Selector to 'TIMING B-C' (marked in red on the panel).

(iii) Carry out procedures (b) and (c) of Section 2.6.2. above.

(iv) If the timing sequence is to be started by a pulse, set the START switch to '+' or '-', according to the polarity (with respect to chassis earth) of the start pulse.

Similarly, if the Stop action is to be controlled by a pulse, make the appropriate adjustment to the STOP switch.

(v) To start the gating time apply a Start signal to the coaxial socket marked 'B' or momentarily depress the START toggle. To end the gating time apply a Stop signal to the coaxial socket marked 'C' or momentarily depress the STOP toggle. Alternatively, should single line gate control be required, the Start and Stop inputs may be linked together (i.e., centre pins of sockets B and C linked together).

In such a case two successive signals presented after occurrence of the reset action and applied between the link and chassis-earth, will cause the gate to open and close respectively.

Youtube.com/TonyAlbus
73 Tony PE1ONS

External leads to inputs B and C should be screened and kept as short as practicable to minimise pick-up which might otherwise cause unwanted trigger operation.

Where practicable, circuits used to trigger the B and C inputs should be battery powered in order to eliminate the possibility of the instrument being triggered by spurious mains-initiated pulses or ripple.

Again, the decimal point is appropriately positioned so that the display, together with any overflow, indicates the time measurement in terms of the timing units selected by the Range switch.

2.7. COUNT

2.7.1. Principle of Operation

In this function the gate is opened and closed by signals applied at the B and C input sockets respectively, or by depression of the START and STOP toggles to their "MANUAL" positions.

During the gating time, signals received at input-A pass via the gate to the counter/display circuit.

2.7.2. Measurement Procedure

Carry out procedures (i) to (v) inclusive, of Section 2.4.2; then proceed as follows -

(a) Set the Function Selector to 'COUNT' A/B-C'.

(b) Momentarily depress the Reset push-button.

(c) To start and stop the gating operation see Section 2.6.3.(iv) and (v).

Providing the count capacity is not exceeded, the resultant display shows the total number of A-input signals received during the gating time.

2.8. STANDARD FREQUENCY OUTPUT

When the Function Selector is set to 'FREQUENCY', signals (as specified in Section 1.2.9.) derived from the internal reference oscillator (or from an external 1 MHz reference source) are available at the front-panel-mounted socket marked 'STD. FREQ'S'; the signal frequency being dependent upon the setting of the Range switch as indicated below.

The signals are momentarily interrupted whenever reset action is initiated.

Range switch positions (clockwise order)	Standard Frequency Output
1	1 MHz
2	100 kHz
3	10 kHz
4	1 kHz
5	100 Hz
6	10 Hz
7	1 Hz
8	0.1 Hz

Since the 'STD. FREQ'S' socket is fed by the output of the internal frequency divider, signals are also produced at this socket for other settings of the Function Selector but they are then dependent upon the gating operations and/or the signal input frequency. On MULTI-PERIOD, the divider is fed by A-input signals (received via an internal pulse shaper); on both TIMING functions it is fed, only during the gating period, by the oscillator output frequency (normally 1 MHz). For these functions the signal frequency at the output socket is -

$$\frac{\text{The divider input frequency}}{\text{Range Switch setting (blue figures)}}$$

On the COUNT function the divider is unused; therefore no output signals are provided at the 'STD. FREQ'S' socket.

2.9. EXTERNAL REFERENCE FACILITY

When the rear-mounted Crystal Reference switch is set to 'INT' the internal 2 MHz oscillator is employed as the reference source and signals from the oscillator are then present at the coaxial socket marked 'EXT'. When the latter setting is used, no external signals should be applied at the 'EXT.' socket, otherwise the instrument will not function correctly due to multiple trigger operation by the two timing signal sources.

When the switch is set to 'EXT', the internal oscillator is switched out of circuit and signals applied to the Crystal Reference socket (as specified in Section 1.2.7) serve as reference signals for the instrument.

This facility may be used to increase the accuracy of the instrument for the standard functions (i.e., by use of a 1 MHz source frequency whose accuracy is superior to that of the internal crystal: see Section 1.2.2) or to alter the significance of the readout so that the instrument will operate in a non-standard manner (i.e., by use of an external source frequency other than 1 MHz).

The facility may be used for frequency ratio measurement as treated in the following section.

2.9.1. Frequency Ratio Measurement

Frequency ratio measurement of signals from two sources may be conducted when the Crystal Reference switch is set to 'EXT'. Signals from one source should be applied to the Crystal Reference socket; those from the second source should be applied to the A-input socket.

The measurements may be conducted with the Function Selector set to FREQUENCY or MULTI-PERIOD, the two functions will be treated separately.

Procedures (ii), (iii), (iv) and (v) of Section 2.4.2, which relate to the use of Display Time and A-input controls and to data logging facilities, are applicable in the following functions.

(a) Frequency Function

With the Function Selector set to FREQUENCY, signals (of frequency f_1) applied to the EXT Crystal Reference socket pass via a frequency divider chain to the internal gate control circuit. The gate is held open while a number of pulses, equal to the division factor of the chain, is received at the 'EXT' input socket. The division factor is indicated by the setting of the Range switch (blue scale) and is selectable in decade steps from 1 to 10^7.

During the gating period, signals (of frequency f_2) applied to signal input A pass via the gate to the counter.

The Displayed Count = $\frac{f2}{f1}$ x division factor

Example:

With f1 = 80 kHz ; f2 = 20 kHz ; Function Selector set to FREQUENCY and Range switch set to 10^4 the displayed count would be 2500.

Therefore

$$2500 = \frac{f2}{f1} \times 10^4$$

The ratio f1 : f2 is therefore given by -

$$\frac{\text{Division factor}}{\text{Count}} : 1$$

i.e., $\frac{10^4}{2500} : 1$

or $4 : 1$

(b) Period Function

With the Function Selector set to MULTI-PERIOD, signals (of frequency f1) applied to the EXT Crystal Reference socket pass via the gate to the counter during the gating time.

The gate is controlled by signals (of frequency f2) applied at input socket A. The signals pass via a frequency divider chain to the internal gate control circuit. The gate is held open while a number of pulses, equal to the division factor of the chain, is received at input A. The division factor is indicated by the setting of the Range switch (i.e., 1 to 10^7 in decade steps).

The Displayed Count = $\frac{f1}{f2}$ x division factor

Example:

With f1 = 80 kHz; f2 = 20 kHz; Function Selector set to MULTI-PERIOD, Range switch set to 10^3 the displayed count would be 4000.

Therefore

$$4000 = \frac{f1}{f2} \times 10^3$$

The ratio f1 : f2 is therefore given by -

$$\frac{\text{Count}}{\text{Division factor}} : 1$$

i.e., $\frac{4000}{10^3} : 1$

or $4 : 1$

When using either function ('a' or 'b' above) the Range switch setting used should be such that the capacity of the counter is not exceeded. In general, maximum accuracy is achieved wh

the displayed count is the greatest obtainable without exceeding the count capacity.

2.10. DATA LOGGING OUTPUT FACILITY

This facility is an optional extra and is provided only if initially ordered. This special version is identified as type TF 2414A/1. The output is provided at a 36-pin Amphenol socket mounted adjacent to the Crystal Reference switch on the rear panel.

For each digit, information is presented in 1.2.4.8 binary coded decimal, (b.c.d).

Pin Connections

Pin connections at the 36-pin Amphenol socket are as follows -

Note: M.S.D. = Most significant digit
L.S.D. = Least significant digit

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	MSD Line 1	13	3rd MSD Line 4	25	Unused
2	MSD Line 2	14	3rd MSD Line 8	26	LSD Line 1
3	MSD Line 4	15	Unused	27	LSD Line 2
4	MSD Line 8	16	4th MSD Line 1	28	LSD Line 4
5	Unused	17	4th MSD Line 2	29	LSD Line 8
6	2nd MSD Line 1	18	4th MSD Line 4	30	Unused
7	2nd MSD Line 2	19	4th MSD Line 8	31	External Reset 1
8	2nd MSD Line 4	20	Unused	32	External Reset 2
9	2nd MSD Line 8	21	5th MSD Line 1	33	Print Command O/P
10	Unused	22	5th MSD Line 2	34	Chassis-earth
11	3rd MSD Line 1	23	5th MSD Line 4	35	+ 6v
12	3rd MSD Line 2	24	5th MSD Line 8	36	External 'Hold'

For the signal specification refer to Section 1.2.10

The data logging outputs are provided by the count-storage circuits; therefore, for 'ON' settings of the Memory switch, the recording time of logging equipment may extend up to the end of the subsequent gating period.

The External reset conditions for Pins 31 and 32 are as follows -

Pin 31 - Contact closure between pins 31 and 35.
Pin 32 - Negative pulse, minimum pulse amplitude 1.0V, maximum pulse amplitude 20V, minimum pulse width 0.2µs.

Chapter 3

Maintenance

3.1. CASE REMOVAL

CAUTION: Whenever the instrument is operated with the case removed, care should be exercised to ensure that no physical contact is made with exposed connections, particularly those of the mains circuit in the regions of the Power switch and power unit.

Each section of the case is secured by one 4BA screw at each side. To remove a section, withdraw both fixing screws, slide the cover backwards sufficiently to disengage the front-edge from the panel surround, then lift away.

3.2. FUSE REPLACEMENT

The instrument should be switched off before replacement of any fuse.

The Mains fuse is housed in a screw-type holder fitted in the rear panel of the instrument.

Fuses associated with the d.c. outputs of the power supply unit are provided on the unit itself. To gain access to these, first remove the top section of the instrument case (see Section 3.1), then the cover-plate of the power unit. Each fuse is mounted on the printed circuit board directly beneath its corresponding marking (e.g., 100mA) on the cover-plate.

3.3. CHECKING AND ADJUSTMENT OF D.C. SUPPLIES

The low voltage d.c. supplies from the 66/210 Unit are preset to +6V and -6V by the potentiometers RV1 and RV2 respectively, mounted under the corresponding markings on the Unit cover-plate. If re-adjustment of these controls is necessary, access may be gained in the same way as for the d.c. supply fuses (see Section 3.2). The high voltage d.c. supply (+235V) is not adjustable since stabilization is unnecessary.

The d.c. voltages can be measured at certain pins on the chassis-mounted 16-way sockets, which are accessible when the lower half of the case is removed. The supply leads to these pins are colour-coded as follows -

Red	:	+6V	Black	:	0V
Violet	:	-6V	Yellow	:	+235V

The recommended test points for these voltages are given in the instructions below.

To check and adjust the positive and negative 6 volt supplies -

(i) Connect a voltmeter between the chassis (-ve probe) and pin 2 (+ve probe) of the right-most socket, as viewed from the chassis under-side-front. Adjust RV1, if necessary, to indicate 6.0V on the meter. The pins are coated with inspection paint, therefore ensure that good connections are made by the voltmeter probes.

If the meter reads 0V, switch off the mains and check the mains fuse. If the latter is intact, check the fuses FS2 and FS3 (see section 3.2.).

(ii) Connect the voltmeter between the chassis (+ve probe) and pin 1 (-ve probe) of the same socket. Adjust RV2, if necessary, to indicate 6.0V on the meter.

If the meter reads 0V, switch off the mains and check the fuses FS2 and FS3.

(iii) Repeat (i) and (ii) until no further adjustment of RV1 and RV2 is necessary to obtain the required voltages.

(iv) Disconnect the meter. Switch off the mains supply before re-assembling the instrument.

To check the +235V supply -

Connect a voltmeter between the chassis (-ve probe) and pin T (+ve probe) of any counter board socket. The meter should read between 212V and 258V. If the meter reads 0V, switch off the mains and check the mains fuse. If the latter is intact, check fuse FS1 (see Section 3.2).

3.4. ADJUSTMENT OF THE PRESET OSCILLATOR-TRIMMER

An oscillator trimmer-capacitor is mounted on the base-plate of the instrument behind the Crystal Reference switch and adjacent to the crystal oven. This control permits adjustment to compensate for the normal ageing process.

The oscillator frequency (2 MHz) may be monitored at the front-panel-mounted TEST socket when the Crystal Reference switch is set to 'INT'. The monitored frequency should be compared with an appropriate external standard frequency and the trimmer adjusted if necessary.

Adjustment of the trimmer should not be made until the instrument has been operated for a period of at least 15 minutes (i.e., when sufficient time has elapsed for temperature stabilization of the Crystal oven).

3.5. DIGITAL INDICATOR AND PRINTED CIRCUIT-BOARD REPLACEMENT

The neon indicator tubes are wired to printed circuit plug-in counter/display boards. It is recommended that, in the event of failure of an indicator, or of a fault having been traced to a plug-in circuit board, the board concerned be removed and returned to Marconi Instruments Limited or Distributor for rectification.

A finger-grip/Spacer is fitted at the top of each plug-in printed circuit board; the particular colour identifies the board type. Guides for the boards are fitted to the mechanical structure of the instrument and are correspondingly coloured so that for board re-insertion, appropriate positions are readily discernible.

For stage layout, see diagram S66/90.

3.6. DECIMAL POINT LAMP REPLACEMENT

The decimal point lamps should be illuminated in turn when (with the Function Selector set to FREQUENCY) the Range switch is set to 10^2, 10^3 and 10^4 consecutively.

Should a decimal point neon lamp fail to function, note the position of the faulty lamp, switch OFF and disconnect the supply; then proceed as follows -

(i) Remove the top half of the case (see Section 3.1).

Youtube.com/TonyAlbus
73 Tony PE1ONS

(ii) Remove the knobs of the Function Selector and Range switch. Each is secured by two grub screws.

(iii) Remove the four fixing screws of the front panel assembly (these are 'Pozidriv' screws, one situated near each corner of the front panel).

(iv) Lift away the front panel which will expose a sub-panel.

(v) Allow the sub-panel, with its surround, to swing forward about its lower edge. To permit this, the capacitor mounted behind the Sensitivity control may be withdrawn from its retaining clip.

(vi) The decimal point lamp containers (small black hollow rod-like containers) are mounted behind the display screen. At the base of each container two soldering pins serve as terminating points for the supply leads and the wires of the decimal point lamp. Disconnect the wires of the faulty lamp; then fit and connect the replacement lamp - Marconi Part No. Z50398.

(vii) Replace the capacitor referred to in (v) above and re-assemble the instrument.

3.7. MAINTENANCE OF PLUG-IN PULSE SHAPER BOARD TYPE 66/330

Two preset potentiometers (RV1 and RV2) are incorporated in this stage as shown in drawing E67/83. In normal circumstances, no maintenance in respect of these components should be necessary; however, adjustment is treated in the circuit description section provided near the rear of this manual (see Section 5.4).

3.8. COLOUR CODING OF LEADS

On the main circuit diagram E67/86, certain wires bear encircled reference letters and/or numbers (e.g., those on wires from the rotors of switches SA7 and SF2). Within the instrument such leads are correspondingly colour coded so that they may be readily identified and traced through the cable-forms.

The colour code system employed is as follows -

Single-coloured leads:

An encircled letter on the diagram represents a lead of one colour, viz -

A = Red B = Violet

When two or more leads of a particular colour are used they are numbered by means of a coloured sleeve at each end. Sleeve colours used confirm to the standard colour code for resistors. Thus the encircled diagram-reference A1 represents a red lead with a brown sleeve.

Bi-coloured leads:

An encircled reference consisting only of digits represents a bi-coloured lead. Again the standard resistor colour code is used to represent the digits.

Where both digits of a lead-number are identical (e.g., 11, 22, etc.) and are therefore represented by the same colour, the bi-colour system is maintained by the inclusion of the colour Pink; therefore an orange/pink lead corresponds to the number 33.

On each lead, the colour with the lower numerical significance should be read first (e.g., a blue/red lead should be read as 26, not as 62). However, the order of reading should be reversed if a pink sleeve is carried at the end of the lead.

Chapter 4

Basic system

DESCRIPTION OF CIRCUITRY

4.1. CIRCUIT DIAGRAMS AND PLUG-IN BOARD COMPLEMENT

The main circuit of the instrument is shown on E67/81.

In this diagram, each plug-in stage (including the power supply) is represented by a block containing the stage type number, and, in parentheses, the drawing number of the corresponding circuit diagram. Numbers inside the periphery of the block are the pin numbers of the corresponding chassis-mounted connectors, and are referred to in the text below by the abbreviation TP (for 'termination point'). Each stage is decribed in the Circuit Description Section - see CONTENTS.

The stage complement is as follows -

Type	Title	Colour-code	
66/100	Double Decade	Grey	3
66/140	Decade Divider	Black	1
66/210	Power Supply	-	1
66/330	Pulse Shaper	Red	1
66/520	Oscillator	Green	1
66/630	Gate, Control and Reset	Beige	1
66/710M	Low Speed Counter with Memory	Light Blue	5
66/730	High Speed Counter with Memory	Dark Blue	1
66/740M	High Speed Integrated Counter with Memory	Turquoise	1

The positions of the stages in the chassis are shown on Layout Diagram S66/90 the colours given being those of the finger-grip/spacers for each plug-in printed-circuit board. (To aid in the correct re-placing of boards in the chassis, the spacer/finger-grips on each board correspond in colour to the guides into which the board slots before mating with its chassis-mounted connector. Boards of one type bear the same colour).

4.2. GENERAL CIRCUIT DESCRIPTION

This section treats the general operation of the counter and relates to the main circuit diagram of the instrument. Circuit descriptions for the individual stages follow Section 4.2.7.

The significance of the lead-references which appear on the main diagram is dealt with in Section 3.7.

4.2.1. Mains and Internal Supplies

The mains supply is received at the 3-core cable and is applied via the interference suppressor network L1, L2 and C8, Power switch SJ and fuse FS1 (0.5A) to the Power Supply Unit, type 66/210.

The power unit provides three d.c. supplies:- A +235 V anode-supply (at TP3) for the indicator tubes and decimal point lamps (V1-3), and 6 V positive and negative supplies at pin 1 and pin 2 respectively (voltage levels are with respect to pin 9, i.e., the OV line or chassis-earth). A 12.6 V a.c. output provided between pin 5 and pin 6 serves to power the thermostatically controlled oven which houses the crystal of the internal reference oscillator.

4.2.2. Input (A) Signal Circuit

Signals received at input 'A' are amplified by the Pre-amplifier type 66/004 before passing to TP10 of Pulse Shaper type 66/330.

Positive output pulses at TP6 of the shaper are available at wafer-1 of the function selector SA and are used as gate input signals on functions Frequency and Count. Negative output pulses at TP8 are available at Function Selector wafers 3 and 6 (i.e., SA3 and SA6), where they are selected to control the gate on Function Timing A-A. The pulses are also available at wafer-7 where, for function Multi-period, they are selected to feed a frequency divider chain and stator-1 of wafer-1 of the Range switch SD3.

The Latch signal line is connected to TP5 of stage 66/330.

4.2.3. Reference Signal Circuit

While the CRYSTAL REFerence switch SE is set to INT. (i.e., to position 1) the 2 MHz output from the Oscillator type 66/520 passes from TP8 via C7 to the input of the shaper section of the 66/520 stage at TP10. This signal is also available at SKT E and at the 2 MHz TEST socket SKT D. Since TP14 is connected to the -6V line (see Circuit Description of stage 66/520), frequency halving occurs, so that the output of the stage (when no Inhibit signal is present at TP12) is a 1 MHz rectangular-wave appearing at TP16.

When switch SE is set to EXT, the input to the shaper section may be fed by an externally-generated reference signal applied to the EXT. REF. I/P socket SKT E. In this position SE takes the output of the internal oscillator to chassis-earth to prevent inter-action of signals from the two sources. It also connects TP14 to the +6V line so that no frequency division occurs within the 66/520 stage, thus giving a rectangular-wave output at TP16 of the same frequency as the external reference source.

The 1 MHz pulses from TP 16 serve as gate input ('clock') pulses in timing operations, entering the control stage type 66/630 at TF14. They are also available at wafer SA7, where, for Frequency Measurement, they are selected to feed the Frequency Divider chain (described below) and stator 1 of wafer SD3.

4.2.4. Frequency Divider Chain and Standard Frequency Output

This chain comprises a Decade Divider type 66/140 and three Double Decades type 66/100. It is fed by signals selected by Function Selector wafer SA7.

Outputs of the decades, with respect to the frequency at SA7 rotor, are as follows -

Stator 1 : Frequency as at SA5 rotor	(1 MHz on Frequency Function when the Internal Reference or a 1 MHz External Reference is used)
Stator 2 : Frequency as at SA5 rotor ÷ 10	(100 kHz on Frequency function, etc.)

Stator 3 : Frequency as at SA5 rotor ÷ 10^2 (10 kHz on Frequency function, etc.)

Stator 4 : Frequency as at SA5 rotor ÷ 10^3 (1 kHz on Frequency function, etc.)

Stator 5 : Frequency as at SA5 rotor ÷ 10^4 (100 Hz on Frequency function, etc.)

Stator 6 : Frequency as at SA5 rotor ÷ 10^5 (10 Hz on Frequency function, etc.)

Stator 7 : Frequency as at SA5 rotor ÷ 10^6 (1 Hz on Frequency function, etc.)

Stator 8 : Frequency as at SA5 rotor ÷ 10^7 (0.1 Hz on Frequency function, etc.)

Signals selected by SD3 rotor are available at wafers SA3 and SA6 for use as gate control signals on the functions Frequency and Multi-period. They are also available for use on the Timing functions to feed the counter/display circuit and are fed to the standard frequency output socket SKT C.

4.2.5. Gate and Control Circuits

Stage type 66/630 houses the gate and main control circuits. With the instrument in the reset state, the first negative pulse to occur at SA3 rotor opens the gate, whilst the next negative pulse to occur at SA6 rotor closes it. The sources of these pulses for positions 1 to 3 of the above wafers have been described earlier: for positions 4 and 5, however, the pulses are produced by the polarity selector stage type 66/006, and are produced by momentary depression of the Start and Stop biased toggles, (SB and SC respectively), or upon application of suitable signals at the Start and Stop inputs (SKTA and SKTB respectively).

The input of the gate, TP14, is fed with pulses from the Oscillator; and the gated pulses produced at TP13 are available at wafer SA8 stator 2, where, on the function MULTI-PERIOD, they feed the Counter chain (see Section 6). The gated pulses are also available at wafer SA7 to feed the Frequency Divider chain on both TIMING functions.

4.2.6. Counter Chain and Display

The signals at function selector wafer SA8 (i.e., gated signals on the functions Frequency, Multi-period and Count, or for both Timing functions, signals selected from the frequency divider chain by SD3 rotor) are fed to the counter chain comprising cascade-connected decade counters. Each counter board houses and drives one of the digital indicator tubes used to display the count.

The instrument contains a display Memory facility (Drg. E 67/81) and the counter chain comprises counter boards types 66/740M, 66/730 and 66/710M. Each board contains a decade counter and a count-storage or Memory circuit with a digital indicator. When the Memory switch SH is set to 'OFF', terminal points H of the counter boards are held at earth potential and the memory circuits and the display follow the progression of the count. When the switch is set to 'ON', the count information is passed to the memory and display circuit only when TP11 of stage 66/630 swings negative at the end of a gating period. The information thus acquired by the memory circuit is retained and displayed until new information is received at the end of the next gating period.

The display system includes three decimal point neon-lamps (v1-3). In relation to the counter chain shown at the top of the diagram, the inter-counter spaces as read from the right are occupied by the lamps V3, V2, V1 respectively.

The presentation of a decimal point occurs only on Frequency and the two Timing functions and is controlled primarily by the Function Selector wafer SA2. The appropriate lamp is selected by Range-Switch wafer SB3 (on the Frequency function) or by wafer SB2 (on the Two Timing functions). The selected lamp is illuminated by the +235 V output at pin 3 of the power unit.

No decimal point is presented in the display when the Range switch (SB) is set to the first position.

4.2.7. Display Time and Reset Circuit

The Gate, Control and Reset stage type 66/630 employs the Display Time selector-switch SF, the Display Time control RV1 and the Reset push-button SG.

The reset pulse produced at TP5 (upon depression of push-button SG, or automatically when switch SF is set to 'Auto') is applied to terminal points E of the counter chain so that each counter stage may be reset to the zero condition, however, due to the display storage facility, no change occurs in the display if the Memory switch SH is set to 'ON'.

The pulse also serves to reset the stages of the frequency divider chain. At each stage the pulse is received at TP4 and, depending upon the setting of Function Selector wafer SA5, at either TP5 or TP6. For the functions Frequency and Multi-period, the chain is set to the 9999999 condition so that the first input pulse received (via SA7 rotor) triggers the chain to the zero condition, thereby producing a pulse at SD3 rotor which (supplied via SA3) opens the gate. For both Timing functions the chain is reset to the zero condition. Although on the Count function the divider chain is not employed, it is again reset to zero.

Function selector wafer SA4 serves to hold the unused reset line of the divider chain stages (i.e., TP5 or TP6) at the required - 6 V level.

Chapter 5

Detailed circuit description of sub-units

5.1. PRE-AMPLIFIER TYPE 66/004 (DRG. E67/63)

The pre-amplifier is designed to convert input signals, of amplitude between 10mV and 250V r.m.s., into rectangular output pulses of approximately 850mV peak amplitude.

The input circuit has a sensitivity control RV1 and voltage-limiting diodes MR1, MR2. A field-effect-transistor amplifier (VT1) feeding an emitter-follower (VT2) provides a high input impedance with wide frequency response.

The integrated circuit X1 incorporates two cascaded amplifier stages followed by a Schmitt Trigger stage, the output of the latter being available at the 'SIGNAL O/P' point. Connection of the 'OFFSET ADJUST' point to a d.c. potential, variable through a fraction of a volt about 0V, allows the mark-to-space ratio of the final output to be adjusted. The bias points +Vcc and -Vee require d.c. supplies of +2.4V and -4.0V respectively.

5.2. POSITIVE/NEGATIVE POLARITY SELECTOR TYPE 66/006 (DRG. E67/80)

The selector comprises two identical gated inverting amplifiers. The description is therefore confined to the one shown on the left-hand side of the circuit diagram.

If START CONTROL I/P B (TP3) is open-circuited, while START CONTROL I/P A (TP1) is connected externally to the 0V line, then VT1 acts as a grounded-emitter amplifier, sensitive only to positive pulses applied to the START I/P (TP4).

If however, START CONTROL I/P A is open-circuited, while START CONTROL I/P B is connected to the 0V line, then VT1 acts as a grounded-base amplifier sensitive only to negative pulses applied to the START I/P.

Diodes MR1 and MR2 limit the input signal excursion to between - 6V and + 6V, approximately, at MR4 cathode.

5.3. DOUBLE DECADE TYPE 66/100 (DRG. ES66/29)

In this circuit VT1-8 form the first decade and VT9-16 the second. Since the two decades are identical except for the termination point numbers used for the respective inputs and outputs (these are indicated on the left of diagram ES66/29) circuit description will be confined to the first decade.

The decade comprises four bi-stables (e.g., VT1-2; VT3-4, etc.) and is in the zero condition when transistors VT2, 4, 6 & 7 are conductive. The circuit is triggered by negative-going input signals applied to TP15 and operation is in 1-2-4-8 code.

The table below indicates the state of the decade for each count condition.

For the respective bi-stables, 'o' represents conduction by VT2, 4, 6 & 7.
For the respective bi-stables, '1' represents conduction by VT1, 3, 5 & 8.

Bi-stable	VT1-2	VT3-4	VT5-6	VT7-8
Condition 0 :	o	o	o	o
Condition 1 :	1	o	o	o
Condition 2 :	o	1	o	o
Condition 3 :	1	1	o	o
Condition 4 :	o	o	1	o
Condition 5 :	1	o	1	o
Condition 6 :	o	1	1	o
Condition 7 :	1	1	1	o
Condition 8 :	o	o	o	1
Condition 9 :	1	o	o	1

Between count conditions 0 and 9, whenever the first bi-stable is triggered from '1' to 'o' a negative-going trigger-signal is passed to the next bi-stable; the action is the same for the second and third bi-stables. When the fourth bi-stable is triggered from 'o' to '1' diode MR18, previously reverse-biased, then serves to close diode-resistor gate R9-MR17 & 18. Therefore no trigger signal passes to the second bi-stable at the count transition nine to zero; but the final bi-stable (which is in the '1' state at count condition 9) is triggered to 'o' by the negative-going signal produced at VT2 collector and passed via C16. As the decade thus reverts to the zero count condition, a negative-going output signal is produced at TP13 (VT7 collector).

Three reset lines (common to both decades) are provided. The 'Reset 0' line (TP5) and 'Reset 9' line (TP6) are necessary since opposite states of the first and fourth bi-stables are required to represent the respective count conditions 0 and 9. The remaining bi-stables (2nd and 3rd) are required in the same state for both condition and are connected to the line marked 'Reset' (TP4).

The reset lines are normally held at -6 V with respect to TP3. The decade is set to zero when the 'Reset' and 'Reset 0' lines are momentarily raised positively by more than +4V; it is set to 9 when the 'Reset' and 'Reset 9' lines are momentarily raised positively by more than +4V.

5.4 DECADE DIVIDER TYPE 66/140 (DRG. ES66/36)

The decade comprises four bi-stables (e.g., VT1-2; VT3-4, etc.) and is in the zero condition when transistors VT2, 4, 6 & 7 are conductive. The circuit is triggered by negative-going input signals applied to TP15 and operation is in 1-2-4-8 code.

The table below indicates the state of the decade for each count condition.

For the respective bi-stables, 'o' represents conduction by VT2, 4, 6 and 7.
For the respective bi-stables, '1' represents conduction by VT1, 3, 5 and 8.

Bi-stable	VT1-2	VT3-4	VT5-6	VT7-8
Condition 0 :	o	o	o	o
Condition 1 :	1	o	o	o
Condition 2 :	o	1	o	o
Condition 3 :	1	1	o	o
Condition 4 :	o	o	1	o
Condition 5 :	1	o	1	o

Bi-stable	VT1-2	VT3-4	VT5-6	VT7-8
Condition 6 :	o	1	1	o
Condition 7 :	1	1	1	o
Condition 8 :	o	o	o	1
Condition 9 :	1	o	o	1

Between count conditions 0 and 9, whenever the first bi-stable is triggered from '1' to 'o' a negative-going trigger signal is passed to the next bi-stable; the action is the same for the second and third bi-stables. When the fourth bi-stable is triggered from 'o' to '1' diode MR10, previously reverse-biased, then serves to close diode-resistor gate R9-MR9 & 10. Therefore no trigger signal passes to the second bi-stable at the count transition nine to zero; but the final bi-stable (which is in the '1' state at count condition 9) is triggered to 'o' by the negative-going signal produced at VT2 collector and passed via C16. As the decade thus reverts to the zero count condition, a negative-going 'output signal' is produced at TP13 (VT7 collector).

Three reset lines are provided. The 'Reset 0' line (TP5) and 'Reset9' line (TP6) are necessary since opposite states of the first and fourth bi-stables are required to represent the respective count conditions 0 and 9. The remaining bi-stables (2nd and 3rd) are required in the same state for both conditions and are connected to the line marked 'Reset' (TP4).

The reset lines are normally held at -6V with respect to TP3. The decade is set to zero when the 'Reset' and 'Reset 0' lines are momentarily raised more positive than +4V; it is set to 9 when the 'Reset' and 'Reset 9' lines are momentarily raised more positive than +4V.

5.5. POWER SUPPLY TYPE 66/210 (DRG. E66/98)

Mains:

The mains supply received at the inter-connecting plug, PLA (pin 7 neutral: pin 8 live), is applied to transformer T1 whose twin primary windings should have been appropriately linked for the supply voltage (i.e., series connected for 200/250 V a.c. supplies: parallel connected for 100/125 V a.c. supplies.)

6 V d.c. Supplies:

Two stabilised supplies (+6V at pin 1 and -6V at pin 2 with respect to chassis earth pin 9) are derived from the centre-tapped secondary winding of T1 by means of the full-wave-rectifier/stabilizer circuits MR2 & 3/VT3 - 5 and MR4 & 5/VT1 & 2 respectively.

The reverse breakdown voltage of Zener diode MR6 serves as a reference potential for the +6V stabilizing circuit (VT3-5) whose output may be preset by means of the voltage control RV1. Corresponding components MR7 and RV2 are provided for the -6V stabilizing circuit.

For each stabilizer, the Zener diode chain (e.g., MR6-RV1-R8) is connected between the +6V and -6V lines, rather than between one 6V line and chassis-earth, so that sufficient supply voltage is ensured to maintain the required breakdown condition of the diode.

235V d.c. supply

A 235V d.c. supply presented between pin 3 (positive) and pin 9 (chassis-earth: negative) of plug PLA is derived from the 210V transformer winding by the circuit of rectifier MR1. The output is provided as the anode-supply for the neon digital indicator tubes and the neon decimal point lamps.

12.6V a.c. Output

The output of the 12.6V secondary winding of transformer T1 is available between pins 5 and 6 of plug PLA. It is provided to power the oven of a temperature controlled quartz crystal oscillator.

5.6. PULSE SHAPER TYPE 66/330 (DRG. E67/83)

Beside a pulse shaper, the board accommodates control circuits and d.c. supply and bias lines, for use with Pre-amplifier type 66/004, described on a separate sheet (CD.66/004 Sheet 1).

+20V Supply

An unsmoothed supply of from +200 to + 300V d.c. may be applied to TP16* ('+EHT') to give a 20V zener-stabilized supply.

Offset Adjustment

The open circuit potential at TP14 ('OFFSET ADJUST') is adjustable by RV1 over the range 0±150mV approximately providing a source of offset-voltage for the linear integrated amplifier on stage type 66/004.

+Vcc and -Vee

The voltages +Vcc (TP13) and -Vee (TP12) are available for supplying the output stages of integrated circuits. The setting of potentiometer RV2 determines the values of Vcc and Vee which by the action of zener diode MR2 are maintained at a constant potential difference.

Pulse Shaper and Latch Circuit

The pulse shaper is designed to operate on signals of any frequency up to 40 MHz, having amplitude in the region of $\frac{1}{2}$ to 1V peak-to-peak.

The signal received at TP10 ('SIGNAL I/P') is amplified by VT3, whose trigger level is determined by the setting of potentiometer RV3, which controls the current through VT2. From VT3 collector the signal passes to emitter-follower VT4 whose output feeds both the main gate control circuit and the secondary output circuit. The latter consists of an inverter VT8 whose output (at 'O/P 2') is short-circuited to the OV line whenever a latch signal (of level +3.5V to +6V approximately) is applied to TP9 ('LATCH').

Main Gate Control Circuit

When VT6 is conducting, VT5 acts as an inverter whose output appears at TP5 ('MAIN O/P'). When VT6 is non-conducting, VT5 is 'cut-off' so that the potential at TP5 is +6V. The state of VT6 is dependent on the Gate Control signal applied to TP4, as long as TP6 ('+6V ENABLE') is connected externally to the +6V line. Disconnection of TP6 from this line renders VT6 insensitive to switching of VT7, so that the Gate Control signal is ineffective.

5.7. OSCILLATOR TYPE 66/520 (DRG. E67/82)

In addition to an oscillator this board also accommodates a pulse shaper and a frequency divider.

Oscillator

When a suitable crystal and its trimmer capacitor are connected in series between TP6* and TP7, the circuit containing VT7 and VT8 form a sinewave oscillator. The control RV1 is preset to give maximum undistorted output at TP8 ('OSC. O/P').

Youtube.com/TonyAlbus
73 Tony PE1ONS

Pulse Shaper (and Latch Circuit)

Signals applied to TP10 ('SHAPER I/P') are normally obtained from the oscillator output (TP8), but may be supplied by an external source. The output of the shaper, consisting of rectangular pulses of the same frequency as the input, is available at TP13, provided that the Latch I/P (TP12) is held at about 0V.

The application of a 'Latch Signal' (more positive than +3.5V) to TP12, causes VT5 to short-circuit VT3 collector to the 0V line, so that no output appears at TP13.

Frequency Divider

The output of the pulse shaper is taken to the circuit associated with transistors VT1 and 2, which acts as a bi-stable when TP14 is connected externally to the +6V line, so giving outputs at TP15 and TP16 of half the input frequency.

If frequency division is not required, TP14 may be connected (externally) to the -6V line, when the circuit acts as a cascade-connected amplifier, providing inverted and non-inverted outputs at TP16 and TP15 respectively.

5.8. GATE, CONTROL AND RESET CIRCUIT TYPE 66/630 (DRG. E67/60)

Gate-Control Circuit

The circuit comprises binaries VT7, 8 and VT9, 10, with inter-lock-transistor VT6 and inhibit-transistor VT5. Gate control signals are produced at TP11 from the output of the first binary; during the 'gate open' period, (i.e., between reception of the Start and Stop signals at TP12 and TP10 respectively) VT8 is conducting and TP11 potential is approximately 0V.

On receipt of a positive Reset pulse (obtained from VT17 emitter via R14 and R15) both VT7 and VT9 are made conducting, so that TP11 attains its 'gate closed' potential of approximately +5.5V. The first negative-going pulse edge thereafter received at TP12 (i.e., the Start signal) triggers the first binary to commence the 'gate open' period.

On receipt of a negative-going pulse edge at TP10 (i.e., the Stop signal), the first binary is triggered back to end the 'gate open' period, during which both VT5 and VT6 have been held non-conducting. This switching-on of VT7 triggers the second binary via C25, thereby making VT6 conduct since the latter is dependent on the collector voltage of VT9. Thus, VT7 is rendered insensitive to any further signals that may arrive at TP10 or TP12, until another Reset pulse puts VT9 back into the conducting state.

Transistor VT5 is held conducting only during the presence of a latch signal (produced from VT15 emitter) which is initiated coincident with the Reset pulse but is of longer duration. This ensures that VT7 cannot be triggered until external counter circuits have been reset.

Signal Gate

This circuit contains transistors VT1-4, and is rendered operative when the 'Enable' line (TP15) is connected to a +6V supply.

The control signal, received at TP16, is normally obtained from the Gate Control output (TP11) via an external connection; it passes through a high input-impedance inverting stage (VT1) to operate the control transistor VT2. During the 'gate open' period, TP16 is at approximately 0V so that VT2 is conducting, thereby allowing VT3 to act as an inverting amplifier whose output appears at TP13.

The signal to be gated, received at TP14, passes through emitter-follower stage VT4 and is then differentiated (by C6 and R7), diode MR1 eliminating the negative 'spikes'. The output at TP13 therefore consists of narrow negative pulses corresponding to the positive-going edges of the input signal at TP14.

Display Time Circuit

The 'close gate' signal produces a negative-going voltage change at VT1 emitter, which passes via C15 to trigger the Display Time monostable circuit VT11, VT12. The monostable remains in the unstable condition (i.e., VT11, VT12 cut-off) for the display time, which is dependent on the time constant C16 x (R32 + R33 $+R_{ext}$), where R_{ext} is the external resistance between TP9 and the 0V line. At the end of this period the circuit reverts to the stable state thereby producing at VT12 emitter a negative pulse, which is used to trigger the Latch-Monostable circuit described below.

The Latch Monostable may be triggered independently of the Display Time if TP8 ('HOLD') is connected to the +6V line. In this condition, VT11 is held conducting and cannot be switched via C15. The versions designated TF 2414A/1 and A/3, which are fitted for Data Logging employ this facility to inhibit Reset action during the operating sequence of the printer or other associated peripheral. The Display control is set to 'Infinity' and Reset action is initiated by a contact closure connected between pins 35 and 36 of the data-output socket. See Sections 1.2.10. and 2.10.

Similarly, external Reset action may be initiated by application of a suitable pulse to pin 32 of the same socket.

Latch and Reset Circuits

The Latch pulse is used to suppress the normal operation of certain circuits until they have been reset, thus preventing undesirable transient conditions from arising. It is obtained, via emitter-follower VT15, from one output of the Latch Monostable circuit VT13, 14, which can be triggered by -

(a) The negative-going pulse edges from VT12, emitter, produced at the end of the Display Time, to switch off VT13 via C18 and MR11; or

(b) An externally-produced negative-going pulse edge injected at TP4 (PULSE RESET I/P), to switch off VT13 via C19 and MR11; or

(c) Momentary connection of TP6 to the +6V line (e.g., by depression of a normally-closed push-button connected between TP6 and TP2), to switch on VT14 via C21 and R43.

The Latch pulse has a minimum amplitude of +2.5V, and a width of approximately 20ms, dependent on time constant R40, C23.

When the Latch Monostable is triggered, the voltage drop at VT14 collector passes via capacitor C24 to the Reset Amplifier VT16, 17, thereby producing at VT17 emitter a positive pulse (of width 0.2ms approximately) which is used to reset the Gate Control binaries. This Reset Pulse is also used to reset remote circuits (e.g., decade counters) connected to TP5; such circuits require their reset lines to be maintained at a level of -5.5V approximately, under normal conditions, but to rise to at least +3.5V during resetting. The Reset Amplifier fulfils this by providing, under quiescent conditions, a low resistance path between TP5 and the -6V line, and a high resistance path between TP5 and the +6V line (VT16 and VT17 being respectively 'on' and 'off'); while, for the duration of the Reset Pulse, the reverse holds true (VT16 being 'off' and VT17 'on').

5.9. LOW SPEED COUNTER AND MEMORY TYPE 66/710M (DRG. ES66/89)

Positive-going signals received at terminal point R trigger the integrated circuit X1 which functions as a 1-2-4-8 b.c.d. decade counter.

A positive-going 'carry signal', produced by the decade count transition 9 to 0 is available at terminal point P for application to a subsequent cascade connected counter stage.

The decade provides 1-2-4-8 b.c.d. outputs at pins 5, 4, 3 & 2 respectively; these feed the data inputs of the integrated buffer/memory unit X2. The input information is accepted by the latter stage throughout the interval that terminal point H is held at the 'transfer level' (i.e., approximately OV). When it is held at the 'store level' (i.e., approximately +4V) information in the stage is retained and therefore no change occurs in the memory until a transfer signal is received.

When data logging outputs are required, current limiters R8 to 11 are fitted so that the 1-2-4-8 b.c.d. information at connections 15, 12, 2 & 5 of the buffer/memory stage is made available at terminal points K to N.

The 1-2-4-8 b.c.d. output from connections 13, 10, 4 & 7 of the buffer/memory stage operate the integrated decoder-driver X3. The ten mutually exclusive outputs of the latter stage serve to control the neon digital indicator tube V1 whose +235V anode-supply is received at terminal point T. A numeral-cathode glows, to display the count information within the buffer/memory stage, when its control line swings negative to approximately OV.

The integrated circuits are supplied by approximately +5V obtained via the voltage dropping diode MR1, from a 6V supply received between the terminal points C (OV) and B (+6V). Decoupling is effected by capacitor C1.

The decade is reset to the zero condition upon receipt of a positive pulse (of approximately +5V) at terminal point E. The clamping diode MR2 is employed to protect the integrated decade against negative potentials presented to this terminal point.

5.10. HIGH SPEED COUNTER AND MEMORY TYPE 66/730 (DRG. ES66/90)

Negative-going signals (with respect to terminal point C) received at terminal point R, trigger the integrated circuit X1 which operates as a decade counter and provides 1-2-4-8 b.c.d. outputs at connections 12, 9, 8 & 11 respectively.

The output of connection 11 operates the inverter/amplifier VT3 so that, coincident with the decade count transistion 9 to 0, a positive going 'carry signal' is produced at terminal point P for application to a subsequent cascade connected counter stage.

The b.c.d. outputs of the decade feed the data inputs of the integrated buffer/memory unit X2. The input information is accepted by the latter stage throughout the interval that terminal point H is held at the 'transfer level' (i.e., approximately OV). When it is held at the 'store level' (i.e., approximately +4V) information in the stage is retained, therefore no change occurs in the memory until a transfer signal is received.

Terminal point H may be externally connected to the OV line if storage action is not required; however, with no such connection it is normally held at the 'store level' by the transfer-pulse shaper circuit VT1 and 2. When the transfer-control input, terminal point J, is held at approximately OV, the capacitor C2 is discharged via VT1 & MR3. Transistor VT2 is normally held cut-off, but when terminal point J is taken positively to approximately +5V, C2 charges via R4 and the base of VT2 so that a

narrow negative-going transfer pulse is produced at VT2-collector and new count information is accepted by the buffer/memory unit.

When data logging outputs are required, current limiters R11 to 14 are fitted so that the 1-2-4-8 b.c.d. information at connections 10, 7, 4 & 13 of the buffer/memory stage is made available at terminal points K to N.

Each positive-going signal at VT1-emitter operates the pulse shaper circuit of VT4 which produces a negative-going print command pulse (for the control of remote data logging equipment) at terminal point D.

The 1-2-4-8 b.c.d. outputs from connections 12, 5, 2 & 15 of the buffer/memory stage operate the integrated decoder-driver X3. The ten mutually exclusive outputs of the latter stage serve to control the neon digital indicator tube Vi whose +235V anode-supply is received at terminal point T. A numeral-cathode glows, to display the count information within the buffer/memory stage, when its control line swings negative to approximately OV.

The integrated circuits are supplied by approximately +5V obtained, via a voltage dropping diode MR1, from a 6V supply received between terminal points C (OV) and B (+6V). Decoupling is effected by capacitor C1.

The decade is reset to the zero condition upon receipt of a positive pulse (approximately +5V) at terminal point E. Clamping diode MR2 is employed to protect the integrated decade against negative potentials presented to this terminal point.

5.11. HIGH SPEED INTEGRATED COUNTER AND MEMORY TYPE 66/740M (DRG. E67/85)

Integrated circuits X1 and X3 each comprise two J-K flip-flops. These are interconnected, together with the four 2-input gates in I.C. X2, to form a decimal divider between pin 1 of X1 and pin 8 of X3. This arrangement enables the divider to operate at input frequencies of up to approximately 50 MHz.

The count, in b.c.d. form, is transferred to the Buffer-and-Memory I.C. X4 as long as termination point H is held at the 'Gate Transfer' level of about OV. When this point is at the 'Store' level of about +4V, the memory becomes insensitive to input signals.

The memory has complementary sets of b.c.d. outputs. One set (from pins 4, 7, 10 & 13) feeds the decoder-and-driver I.C. X5, which converts the count into 10-line form for switching the numerical indicator tube V1.

The other set (from pins 2, 5, 12 & 15) may be made available for data-logging by fitting resistors R6 to 9.

The counter may be reset to zero by application of a positive pulse to termination point E, sufficient to momentarily reduce the potential at pins 4 and 10 of X1 and X3 to near OV.

Diode MR1 drops the positive supply voltage to a level of about +5V for the integrated circuits.

Chapter 6

Replaceable parts

Each stage may be supplied fitted with the components specified, or with equivalent types.

6.1. ORDERING INFORMATION

When ordering spare parts, quote the Marconi Instruments FPP Part Number, plus the instrument Type Number, e.g., TF 2414A FPP X12345/67.

Orders may be placed via a Marconi Instruments Agent, or direct to -

Marconi Instruments Limited
Service Division,
Hedley Road,
St. Albans,
Hertfordshire, England.

6.2. PRE-AMPLIFIER TYPE 66/004 (DRG. E67/63)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1	3.9M ohms ±5% ¼W	Carbon	X50501/39
R2,7	47 ohms " "	"	X50500/17
R3,5	1.5k ohms " "	"	X50500/53
R4	4.7k ohms " "	"	X50500/65
R6	6.8k ohms " "	"	X50500/69
R8,13	220 ohms " "	"	X50500/33
R9	2.2k ohms " "	"	X50500/57
R10,11	10k ohms " "	"	X50500/73
R12	270 ohms " "	"	X50500/35
Resistor, Variable			
RV1	1M ohm	Carbon Lin.	X20999/74
Capacitors			
C1	0.47µF ±20%		X23914/24
C2	82pF ±10%	Ceramic	Y50505/12
C3,8,13	0.068µF±10%	Polyester	X23914/54
C4,6,9,11,14,17	1000pF ±10%	Ceramic	Y50509/11
C5,10,12,15,16	33µF (10V)	Electrolytic	Y22776/16
C7	10µF (20V)	Electrolytic	Y22776/17
C18-21	0.047µF $^{+50\%}_{-25\%}$	Ceramic	X23914/55
Diodes	**Type No.**		
MR1,2	IN4009 or equivalent		X20639/31
Transistors			
VT1	MPF 102		X20638/86
VT2	U15718/2 or equivalent (Current gain at least 70)		X20638/55
Integrated Circuit			
X1	MC 1035P		X50520/9
Inductors		**Description**	
L1,2		h.f. choke	Z50524

Sockets	Value	Description	Marconi Part No. TF 2414A FPP/
SKT A		B.N.C.	X50508/4

6.3. POSITIVE/NEGATIVE POLARITY SELECTOR TYPE 66/004 (DRG. E67/80)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,10	100 ohms ±5%¼W	Carbon	X50500/25/P
R2,9	100k ohms " "	"	X50501/1/P
R3,8	10k ohms " "	"	X50500/73/P
R4-7	1k ohms " "	"	X50500/49
Capacitors			
C1,2	4700pF ±10%	Polyester	X23914/40
Diodes	Type No.		
MR1-8	1N4009 or equivalent		X20639/31
Transistors			
VT1,2	U15718/2 or equivalent*		X20638/55

* To be in the same gain group, i.e., to have the same spot colour(s).

6.4. DOUBLE DECADE TYPE 66/100 (DRG. ES66/29)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,8,9,34,41,42	3.3kΩ ±5%¼W HiStab	Carbon	X50500/61
R2,5,11,14,19,22,27,30, 35,38,44,47,52,55,60,63	1kΩ " " "	"	X50500/49
R3,4,12,13,20,21,28,29, 36,37,45,46,53,54,61,62	4.7kΩ " " "	"	X50500/65
R6,7,15,16,23,24,31,32, 39,40,48,49,56,57,64,65	18kΩ " " "	"	X50500/79
R10,17,18,25,26,33,43, 50,51,58,59,66	6.8kΩ " " "	"	X50500/69
Capacitors			
C(1-34)	47pF ±5%	Ceramic N750 LEMCO	Y50505/4
Transistors	Type		
VT(1-16)	BSY65 or 2N706		X20638/52
Diodes			
MR(1-20)	1S44 or BAY36		X20639/31

6.5. DECADE DIVIDER TYPE 66/140 (DRG. ES66/36)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,8,9,10,17,18,25,26, 33	3.3kΩ ±5%¼W HiStab	Carbon	X50500/61
R2,5,11,14,19,22,27,30	560Ω " " "	"	X50500/43
R3,4,12,13,20,21,28,29	2.2kΩ " " "	"	X50500/57
R6,7,15,16,23,24,31,32	10kΩ " " "	"	X50500/73

Youtube.com/TonyAlbus
73 Tony PE1ONS

Capacitors	Value	Description	Marconi Part No. TF 2414A FPP/
C(1-16)	47pF ±5%	Ceramic N750 LEMCO	Y50509/4
Transistors	**Type**		
VT(1-8)	BSY38		X20638/59
Diodes			
MR(1-10)	1S44 or BAY36		X20639/31

6.6. POWER SUPPLY TYPE 66/210 (DRG. E66/98)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1	470kΩ ±5%¼W HiStab	Carbon	X50501/17
R2	330Ω " " "	"	X50500/37
R3	3Ω ±10%3W	Wire wound, Welwyn	Z21092/3
R4	820kΩ ±5%¼W HiStab	Carbon	X50500/47
R5	2.2kΩ " " "	"	X50500/57
R6	0.5Ω ±10%3W	Wire wound, Welwyn	Z21092/6
R7	1kΩ ±5%¼W HiStab	Carbon	X50500/49
R(8-10)	1.5kΩ " " "	"	X50500/53
R11	270Ω " " "	"	X50500/35
Resistors Variable			
RV1,2	1kΩ ±20%¼W	Carbon Lin. Plessey	X20999/58
Capacitors			
C1	8µF(350V)	Electrolytic, Hunts	Y20643/50
C2	0.1µF(400V)	Polyester, Mullard	X23914/45
C3	4000µF(25V)	Electrolytic, Mullard	X20643/51
C4	1250µF(25V)	Electrolytic, Mullard	X20643/52
C5,6	120µF(16V)	Electrolytic, Mullard	Y50506/10
C7,8	1000pF ±10%	Ceramic (High K), Erie	Y50509/11
C9,10	8µF(10V)	Electrolytic, Mullard	Y50506/2
Diodes	**Type**		
MR1	BYX10	Mullard	X20639/35
MR(2-5)	IN4001	Mullard	X20639/45
MR6,7	BZY88/C4V7	Mullard	X20639/33
Transistors			
VT1	2N4037	R.C.A.	X20638/82
VT2	V435	Fairchild	X20638/72
VT3,4	U15718/2	Fairchild	X20638/55
VT5	40250	R.C.A.	X20638/60
Fuses	**Rating**		
FS1	100mA		Z26413/1
FS2,3	1.5A		Z26413/2

Transformer		Marconi Part No. TF 2414A FPP/
T1		Y51043

Plug	Type	
PLA	B9A	Z50402

6.7. PULSE SHAPER TYPE 66/330 (DRG. E67/83)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,2	22kΩ ±5% 1W	Carbon	X20652/32
R3,4	6.8kΩ ±5% ¼W HiStab	"	X50500/69/P
R5,15	330Ω " " "	"	X50500/37/P
R6,31	1kΩ " " "	"	X50500/49/P
R7	75Ω " " "	"	X50500/22/P
R8	2.7kΩ " " "	"	X50500/59/P
R9,28	5.6kΩ " " "	"	X50500/67/P
R10,12,16,21,23,25,30	47Ω " " "	"	X50500/17/P
R11	100Ω " " "	"	X50500/25/P
R13,14,19	390Ω " " "	"	X50500/39/P
R17	220Ω " " "	"	X50500/33/P
R18,24	2.2kΩ " " "	"	X50500/57/P
R20	47kΩ " " "	"	X50500/89/P
R22	12kΩ " " "	"	X50500/75/P
R26	820Ω " " "	"	X50500/47/P
R27	33kΩ " " "	"	X50500/85/P
R29	4.7kΩ " " "	"	X50500/65/P
R32	3.3kΩ " " "	"	X50500/61/P
Resistors Variable			
RV1,2	560Ω		X20999/61
RV3	5.6kΩ ±20% ¼W	Carbon Plessey	X20999/55
Capacitors			
C1	8µF (150V)	Electrolytic	X20643/57
C2	100µF (4V)	Electrolytic	Y50506/5
C3,4,6,8,11,14,16,17	0.047µF +50% -25%	Ceramic	X20641/55
C5,7,9,12	12.5µF (6.4V)	Electrolytic	Y50506/3
C10,13,15	22pF ±10%	Ceramic	Y50509/2

Diodes	Type	
MR1	BZY88C2C	X20639/51/P
MR2	BZY88C5V6	X20639/30/P
MR3,4	IN4009	X20639/41/P

Transistors			
VT1	BC108	Mullard	X20638/71
VT2-9*	U15718/2 or equivalent	Fairchild	X20638/55

* VT2,3 to have matched gain (i.e., the same colour spot), over 70
VT4,5 to have gains of over 70.

6.8. OSCILLATOR TYPE 66/520 (DRG. E67/82)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,3,4,7,12	2.2kΩ ±5% ¼W HiStab	Carbon	X50500/57
R2,5,19	470Ω " " "	"	X50500/41
R6,8,15,16,25	22kΩ " " "	"	X50500/81

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R9	8.2kΩ ±5% ¼W HiStab	Carbon	X50500/71
R10	680Ω " " "	"	X50500/45
R11,20	1kΩ " " "	"	X50500/49
R13,28,32	10kΩ " " "	"	X50500/73
R14,29	100Ω " " "	"	X50500/25
R17 30	3.3kΩ " " "	"	X50500/61
R18	5.6kΩ " " "	"	X50500/67
R21	33kΩ " " "	"	X50500/85
R22	150kΩ " " "	"	X50501/5
R23	47kΩ " " "	"	X50500/89
R24	330Ω " " "	"	X50500/37
R26	68Ω " " "	"	X50500/21
R27	15kΩ " " "	"	X50500/77
R31	27kΩ " " "	"	X50500/83
R33,34	47Ω " " "	"	X50500/17
Resistor Variable			
RV1	5.6kΩ ±20% ¼W	Carbon Lin, Plessey	X20999/55
Capacitors			
C(1-4)	47pF ±5%	Ceramic N750, Erie	Y50509/4
C5	56pF ±5%	Ceramic N750, Erie	Y50509/5
C6,8	22pF ±10%	Ceramic N220, Erie	Y50509/2
C7	8µF (10V)	Electrolytic, Mullard	Y50506/2
C9,11,17,18,20,22	0.068µF ±10%(250V)	Polyester, Mullard	X23914/54
C10	0.0047µF ±10%	Metallised Film, Hunts	X23914/40
C12	1000µF ±1%	Polyester, Mullard	X23914/41
C15	82pF ±5%	Ceramic N560, Erie	Y50509/6
C19,21	12.5µF (6.4V)	Electrolytic	Y50506/3
Transistors	**Type**		
VT1,2,5,7	U15718	Fairchild	X20638/55
VT3,4,8	BSY95A	S.T.C.	X20638/56
VT6	BC108	Mullard	X20638/71

Note: VT1 and 2 to be matched, i.e., to have same colour spot.
VT3 and 4 to be matched, i.e., to have same colour spot.

Diodes			
MR1	IN4009	Fairchild (1 S44)	X20639/31

6.9. GATE CONTROL AND RESET TYPE 66/630 (DRG. E67/60)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,38	5.6kΩ ±5% ¼W HiStab	Carbon	X50500/67/P
R2	33kΩ " " "	"	X50500/85/P
R3,15,24	820Ω " " "	"	X50500/47/P
R4,37,53	47Ω " " "	"	X50500/17/P
R5,20,36,42,49	2.2kΩ " " "	"	X50500/57/P
R6,26,28	680Ω " " "	"	X50500/45/P
R7,8	470Ω " " "	"	X50500/41/P
R9	100Ω " " "	"	X50500/25/P

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R10,11	47kΩ ±5% ¼W HiStab	Carbon	X50500/89/P
R12,21-23.31,32,43,52	4.7kΩ " " "	"	X50500/65/P
R13,19	390Ω " " "	"	X50500/39/P
R14,18,44,46,47	1kΩ " " "	"	X50500/49/P
R16,17,25,27	3.3kΩ " " "	"	X50500/61/P
R29,30,40,45	15kΩ " " "	"	X50500/77/P
R33	39kΩ " " "	"	X50500/87/P
R34	330Ω " " "	"	X50500/37/P
R35	18kΩ " " "	"	X50500/79/P
R39	470kΩ " " "	"	X50501/17/P
R41	1.5kΩ " " "	"	X50500/53/P
R48	27kΩ " " "	"	X50500/83/P
R50	33Ω " " "	"	X50500/13/P
R51	10kΩ " " "	"	X50500/73/P
Capacitors			
C1,4,12,14	22pF ±10%	Ceramic	Y50509/2
C2,3,16,26	12.5µF (6.4V)	Electrolytic	Y50506/3
C5,9,13,27	0.068µF ±10%	Polyester	X23914/54
C6	220pF ±10%	Ceramic	Y50509/8
C7,11,25	100pF ± 5%	Ceramic	Y50509/7
C8,10	10pF ± 5%	Ceramic	Y50509/1
C15,18	560pF ±10%	Ceramic	Y50509/10
C17	1000pF ±10%	Ceramic	Y50509/11
C19,21	0.01µF ±10%	Polyester	X23914/34
C20	0.047µF ±10%	Polyester	X23914/38
C22	33pF ± 5%	Ceramic	Y50509/3
C23	2µF (40V)	Electrolytic	Y50506/1
C24	0.022µF ±10%	Polyester	X23914/37
Diodes	**Type**		
MR1-11	IN4009 or equivalent		X20639/31/P
MR12	IN4009	Fairchild	X20639/41/P
Transistors			
VT1-6,11,13-17*	U15718/2 or equivalent		X20638/55
VT7-10*	U15718/2 or equivalent	Fairchild	X20638/55
VT12	V435	Fairchild	X20638/72

Note: Transistors supplied by Marconi Instruments Limited for use in TF 2414A are marked on their cases by coloured spots according to their current gains. The following colour code is used -

Current Gain	Colour
28-40	Red
41-50	Yellow
51-60	Green
61-70	White
71-90	Pink
91-110	Pink & Yellow
111-150	Pink & Green
151-170	Pink & White
Over 170	Pink, White & White

* VT7 & VT8 to be matched, i.e., to have the same colour spot
VT9 & VT10 " " " " " " " " " "
VT13 & VT14 " " " " " " " " " "
VT16 & VT17 " " " " " " " " " "

Youtube.com/TonyAlbus
73 Tony PE1ONS

6.10. LOW SPEED COUNTER AND MEMORY TYPE 66/710M (DRG. ES66/89)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1	33kΩ ±2% ½W HiStab	Carbon	X50512/1
R2,7	2.2kΩ ±5% ¼W "	"	X50500/57
R(8-11)	1kΩ " " "	"	X50500/49
Capacitor			
C1	0.1µF ±10%(250V)	Polyester, Mullard	X23914/27
Diodes	**Type**		
MR1	U2973/2	Fairchild (1 S44)	X20639/31
MR2	IN4009	Mullard	X20639/41
Integrated Circuits			
X1	CµL9958	Fairchild	Z50520/7
X2	CµL9959	Fairchild	Z50520/6
X3	CµL9960*	Fairchild	Z50520/8
Display Tube			
V1	XN12	Hivac	Z50391/1

* Specially selected and available under the Marconi part number quoted.

6.11. HIGH SPEED COUNTER AND MEMORY TYPE 66/730 (DRG. ES66/90)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1,2,4,5,8,9	2.2kΩ ±5% ¼W HiStab	Carbon	X50500/57
R3	470Ω " " "	"	X50500/41
R6,(11-14)	1kΩ " " "	"	X50500/49
R7	8.2kΩ " " "	"	X50500/71
R10	33kΩ ±2% ½W "	"	X50512/1
R15	3.3kΩ ±5% ¼W "	"	X50500/61
Capacitors			
C1	0.1µF ±10%(250V)	Polyester, Mullard	X23914/27
C2,4	560pF ±10%	Ceramic (High K), Erie	Y50509/10
C3	0.01µF ±10%(250V)	Polyester, Mullard	X23914/34
Diodes	**Type**		
MR1,3,4	U2973/2	Fairchild (1 S44)	X20639/31
MR2	IN4009	Mullard	X20639/41
Transistors			
VT1	V435	Fairchild	X20638/72
VT2,3	U15718/2	Fairchild (2N2369)	X20638/55
VT4	BC108	Mullard	X20638/71
Integrated Circuits			
X1	SN7490N	Texas	Z50520/5
X2	CµL 9959	Fairchild	Z50520/6
X3	CuL 9960*	Fairchild	Z50520/8

* Specially selected and available under the Marconi Part number quoted

Display Tube	Type	Description	Marconi Part No. TF 2414A FPP/
V1	XN12	Hivac	Z50391/1

6.12. HIGH SPEED INTEGRATED COUNTER WITH MEMORY TYPE 66/740M (DRG. E67/85)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1	33kΩ ±5% ¼W HiStab	Carbon	X50500/85/P
R2	4.7kΩ " " "	"	X50500/65/P
R3	22kΩ " " "	"	X50500/81/P
R4,5	2.2kΩ " " "	"	X50500/57/P
R6-9*	1kΩ " " "	"	X50500/49/P
R14	180Ω " " "	"	X50500/31/P
Capacitor			
C1	0.1µF ±10%	Polystyrene	X23914/27
Diode	**Type**		
MR1	IN4009 or equivalent	Mullard	X20639/31/P
Transistor			
VT1	U15718/2 or equivalent	Fairchild	X20638/55
Integrated Circuits			
X1,3	MC 3062		X50520/11
X2	TTµL 9002		X50520/10
X4	CµL 6 9959 79		X50520/6
X5	CµL 6 9960 79**		X50520/8
Display Tube			
V1	XN12		Z50391/1

* Used only with b.c.d. outputs
** Specially selected

6.13. COMPONENTS ON MAIN CHASSIS (DRG. E67/81)

Resistors	Value	Description	Marconi Part No. TF 2414A FPP/
R1	4.7kΩ ±5% ¼W	Carbon	X50500/65
R2,3,5	1kΩ " "	"	X50500/49
R4	330kΩ " "	"	X50501/13
Resistor, Variable			
RV1	500kΩ ±20% 2W	Carbon Lin.	X20999/53 (See SF)
Capacitors			
C1,2,7	0.1µF ±10%	Polyester	X23914/27
C3,4,10,11	0.047µF +50% -25%	Ceramic	X20641/55
C5	47pF ±5%	Ceramic	Y50505/4
C6	4-60pF	Air trimmer	Z21135/5
C8(a+b+c)	(0.1+0.005+0.005)µF	Mains Suppressor	Z26102
C9	0.068µF ±10%	Polyester	X23914/36
C12	0.047µF ±10%	Polyester	X23914/38

Diodes	Type	Description	Marconi Part No. TF 2414A FPP/
MR1,2	IN4009 or equivalent		X20639/31

Switches	Function	Description	Marconi Part No. TF 2414A FPP/
SA	Function Selector	8 pole 5 way rotary (3 section)	Y50677
SB	Start Selector	3 pole 3 way toggle (spring-biased in pos.3)	Z51469
SC	Stop Selector	3 pole 3 way toggle (Spring-biased in pos.3)	Z51469
SD	Range Selector	3 pole 8 way rotary (3 section)	Y50678
SE	Crystal Reference Switch	2 pole 2 way slide	Z27067/1
SF	Display Time Switch	2 pole on/off	X20999/53 (See RV1)
SG	Reset Push-button	1 pair N/O contacts	Z50393
SH	Display Storage Switch	1 pole 2 way toggle	Z51095
SJ	Power Switch	2 pole on/off rocker	Z51468

Sockets	Function	Type	Marconi Part No. TF 2414A FPP/
SKT A,B	Start, Stop inputs	B.N.C.	X50508/4
SKT C	Stand. Freq. output	Wander	X20637/85
SKT D	2 MHz Test output	Wander	X20637/85
SKT E	Ext. reference input	B.N.C.	X20637/96

Terminal			
TP1	Chassis-earth terminal		Y51121

Inductors			
L1,2	Mains Choke		Z4422

(The two chokes are supplied as a pair under this part number)

Neon Lamps			
V1-3	Decimal point lamp 16 L	Hivac	Z50398

Crystal			
XL1	2 MHz frequency		Y20650/11

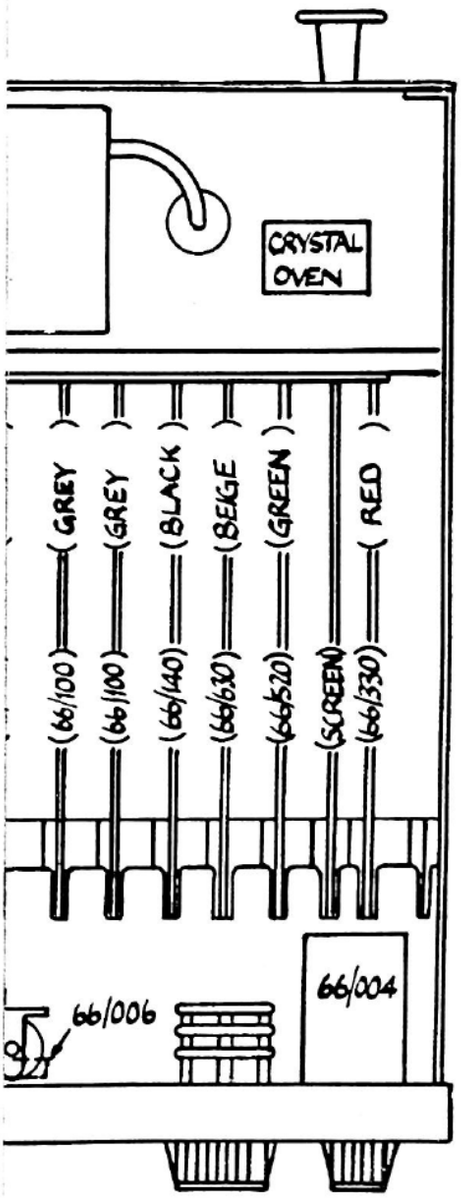
(Mounted in Crystal Oven & socket, Marconi part No. Z50700)

Fuse			
FS1	500mA rating		Z22867/2

For Counters with type nos. TF 2414A/1 & A/3, add -

Data Logging Output socket (to mate with Amphenol plug 57-30360	X20637/80* Z20637/79)

* Mating free plug:- Amphenol 57-30360; Marconi Part No. Z20637/79



GENERAL LAYOUT DIAGRAM

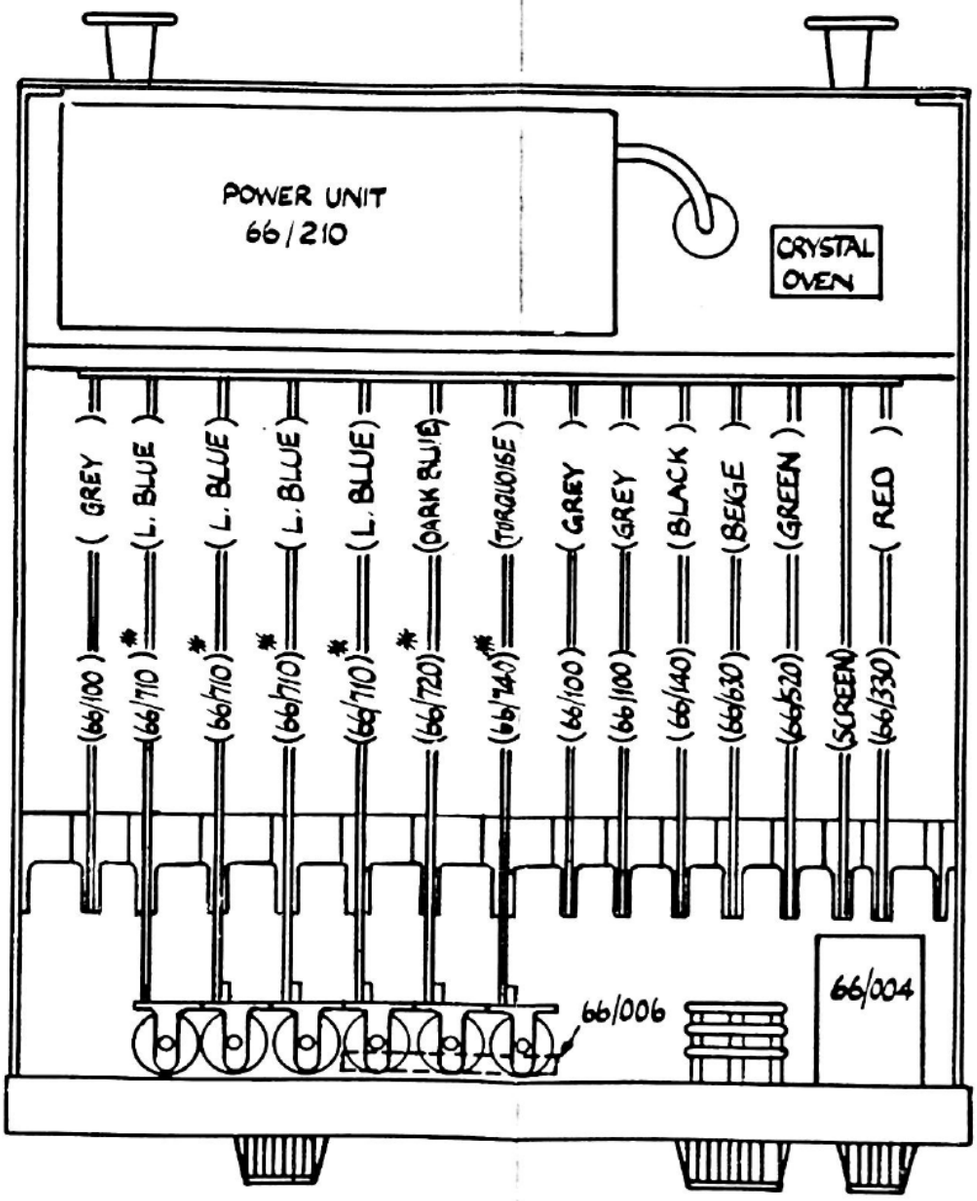
DRG NO S66/90

TF 2414A

COUNTER/TIMER

INSTRUCTION MANUAL

MARCONI INSTRUMENTS LIMITED



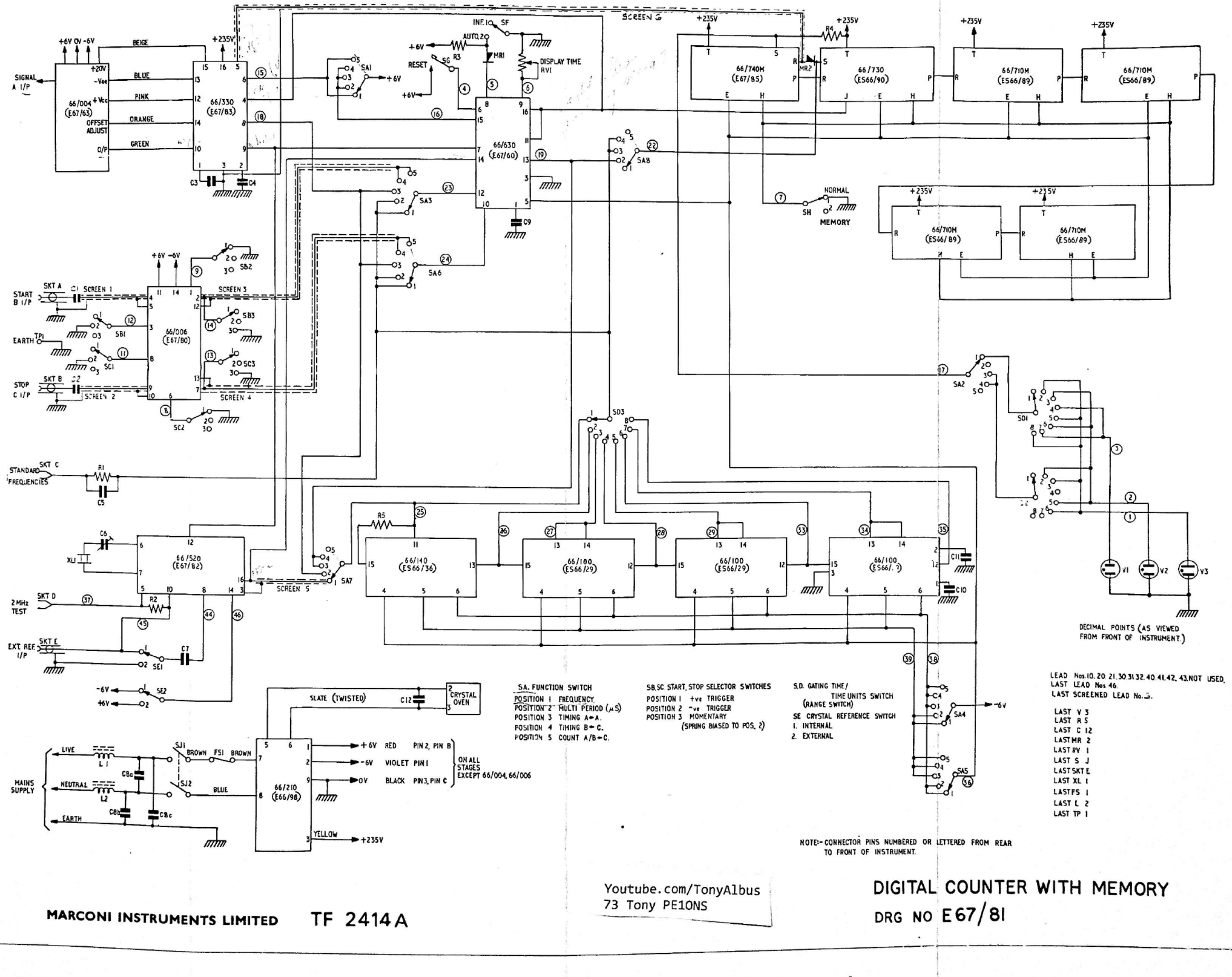
MARCONI INSTRUMENTS LIMITED

TF 2414A

GENERAL LAYOUT DIAGRAM

DRG NO S66/90

Youtube.com/TonyAlbus
73 Tony PE1ONS



SA. FUNCTION SWITCH
POSITION 1 FREQUENCY.
POSITION 2 MULTI PERIOD (μS)
POSITION 3 TIMING A→A.
POSITION 4 TIMING B→C.
POSITION 5 COUNT A/B→C.

SB,SC START, STOP SELECTOR SWITCHES
POSITION 1 +ve TRIGGER
POSITION 2 -ve TRIGGER
POSITION 3 MOMENTARY
(SPRING BIASED TO POS. 2)

S.D. GATING TIME/ TIME UNITS SWITCH (RANGE SWITCH)
SE CRYSTAL REFERENCE SWITCH
1. INTERNAL
2. EXTERNAL

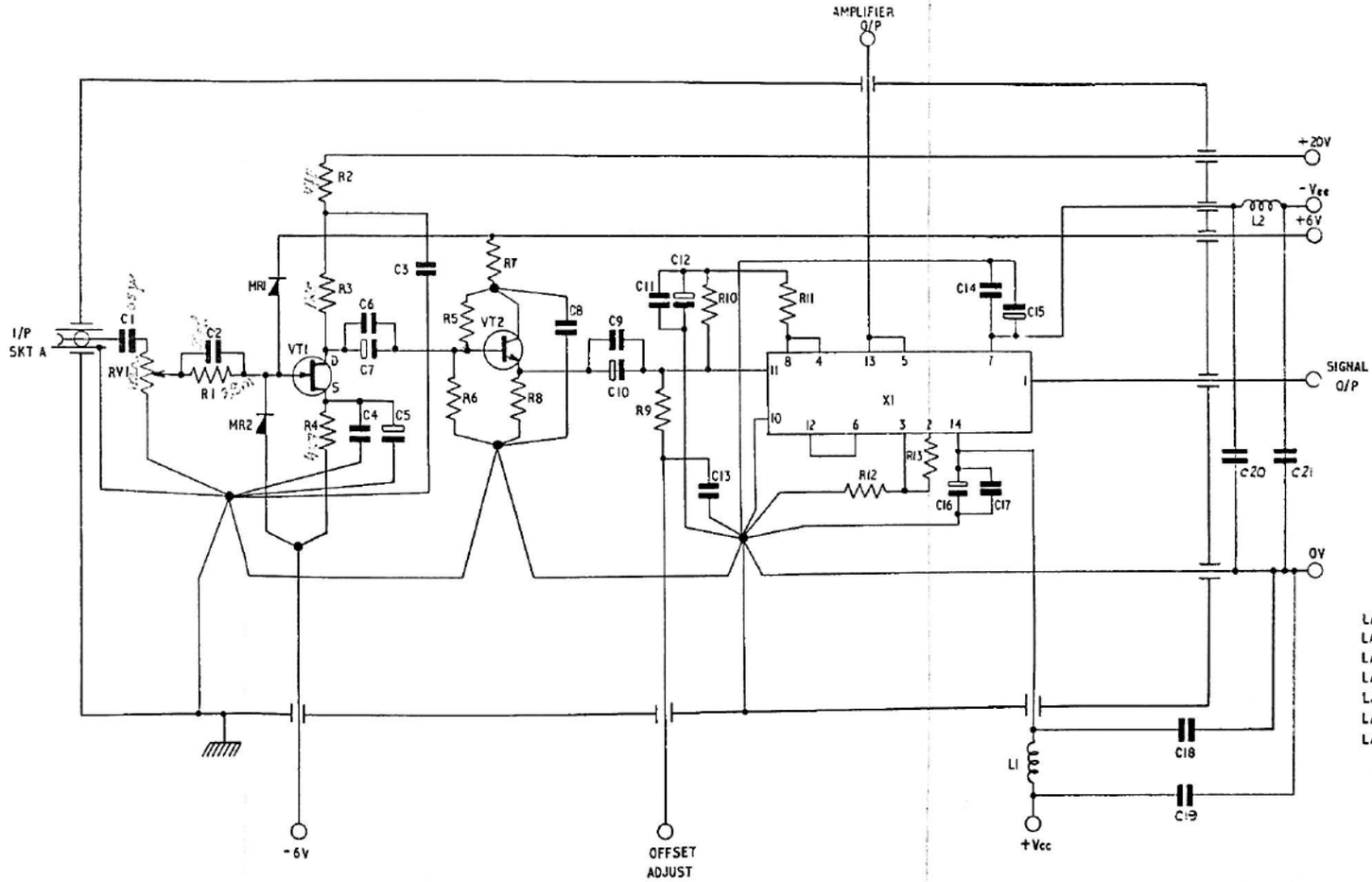
NOTE:- CONNECTOR PINS NUMBERED OR LETTERED FROM REAR TO FRONT OF INSTRUMENT.

Youtube.com/TonyAlbus
73 Tony PE1ONS

MARCONI INSTRUMENTS LIMITED TF 2414A

DIGITAL COUNTER WITH MEMORY

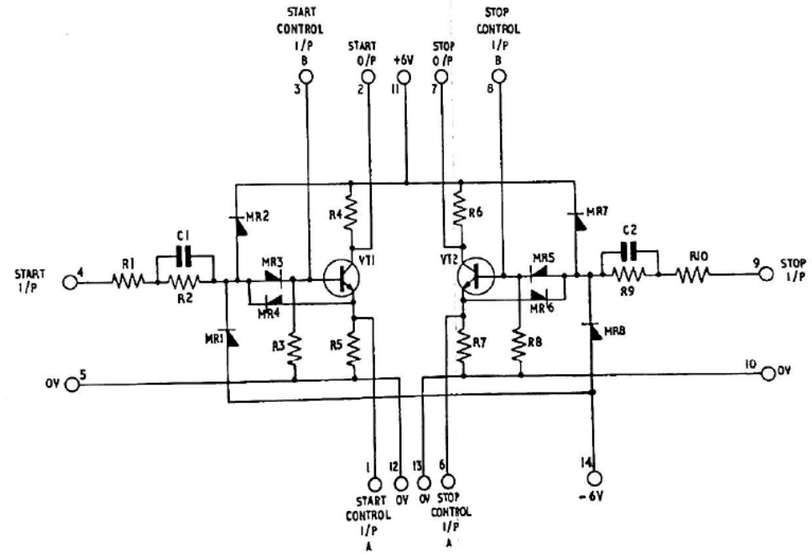
DRG NO E67/81



MARCONI INSTRUMENTS LIMITED TF 2414A

PRE-AMPLIFIER

TYPE 66/004
DRG. NO. E 67/63



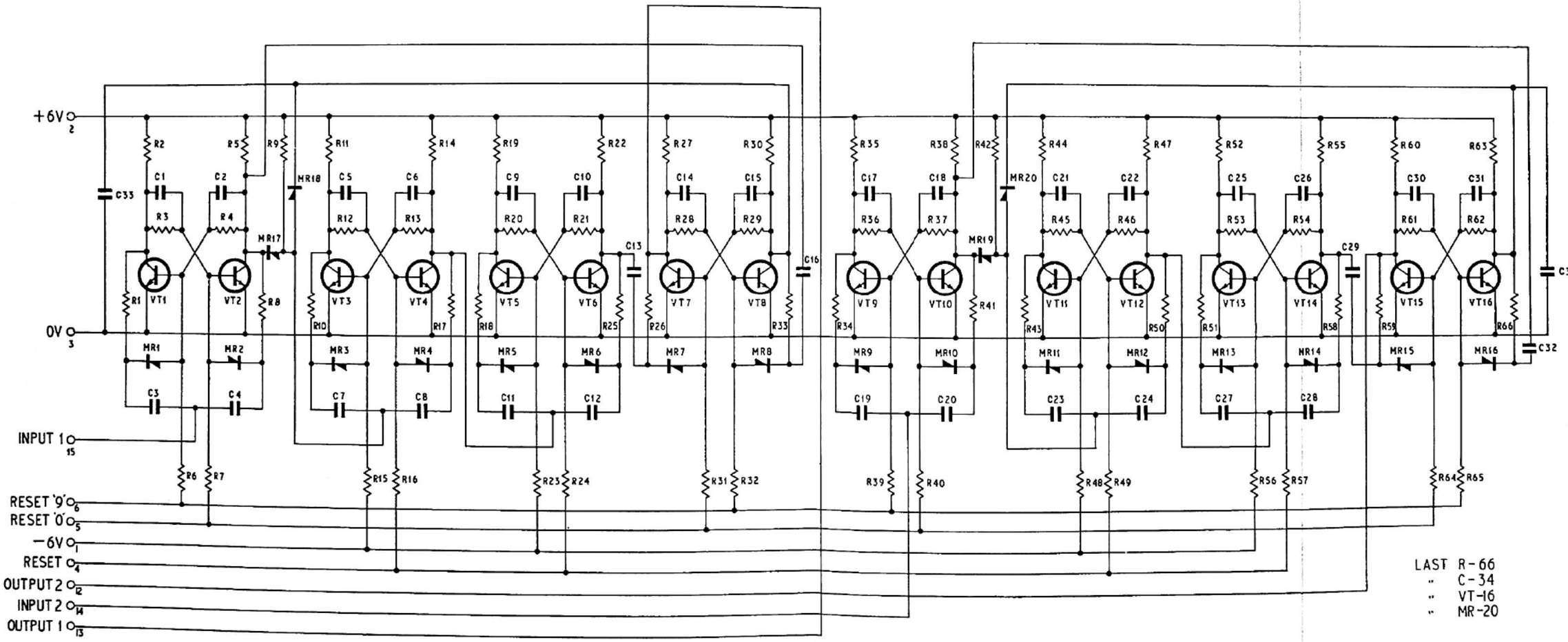
LAST R-10
LAST C-2
LAST MR-8
LAST VT-2

MARCONI INSTRUMENTS LIMITED

TF 2414A

POSITIVE / NEGATIVE POLARITY SELECTOR

TYPE 66/006
DRG. NO. E67/80



LAST R-66
" C-34
" VT-16
" MR-20

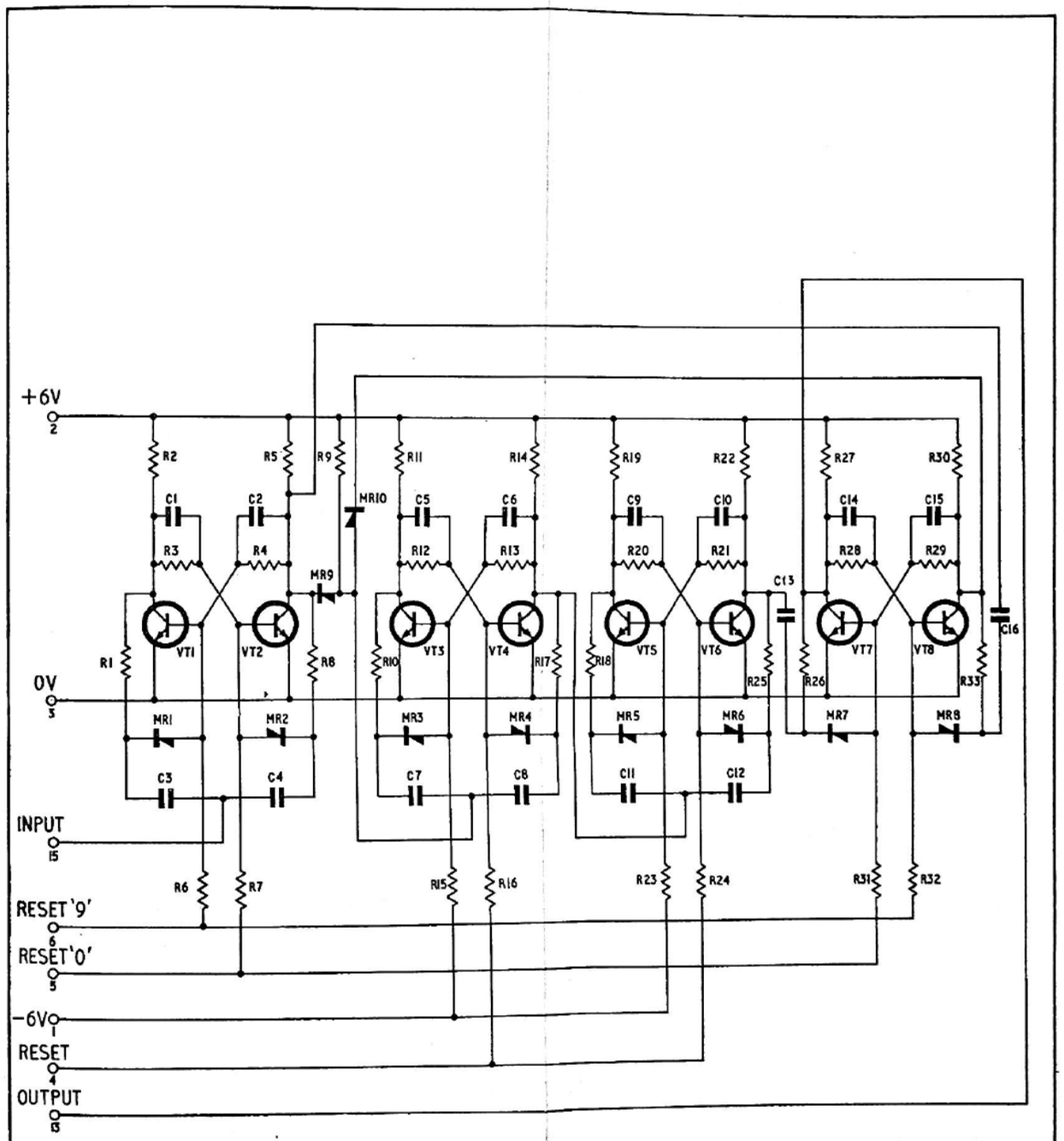
MARCONI INSTRUMENTS LIMITED TF 2414A

DOUBLE DECADE

TYPE 66/100

DRG.NO ES66/29 ISSUE A

Youtube.com/TonyAlbus
73 Tony PE1ONS



LAST R-33
" C-16
" VT-8
" MR-10

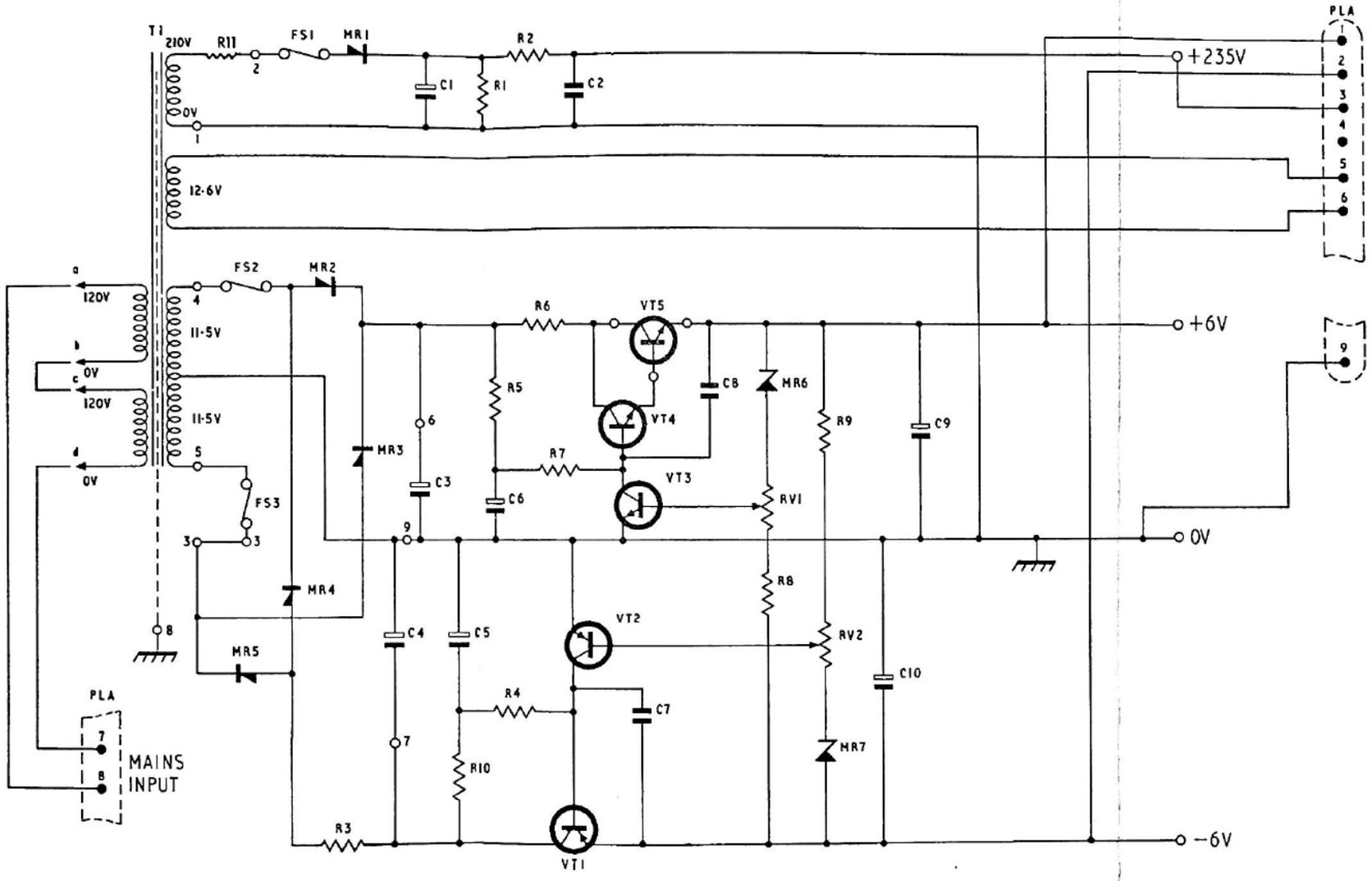
MARCONI INSTRUMENTS LIMITED

TF 2414A

DECADE DIVIDER

TYPE 66/140

DRG.NO ES66/36



LAST R-10
" RV-2
" C-10
- MR-7
" VT-5
" FS-3

NOTES :- CONNECTIONS ARE SHOWN FOR 200/250V WORKING.
FOR 100/125V WORKING DISCONNECT LINK FROM b-c & CONNECT LINKS FROM a TO c AND b TO d.
TERMINATION POINTS ON THE PRINTED CIRCUIT BOARD ARE NUMBERED THUS —o 2

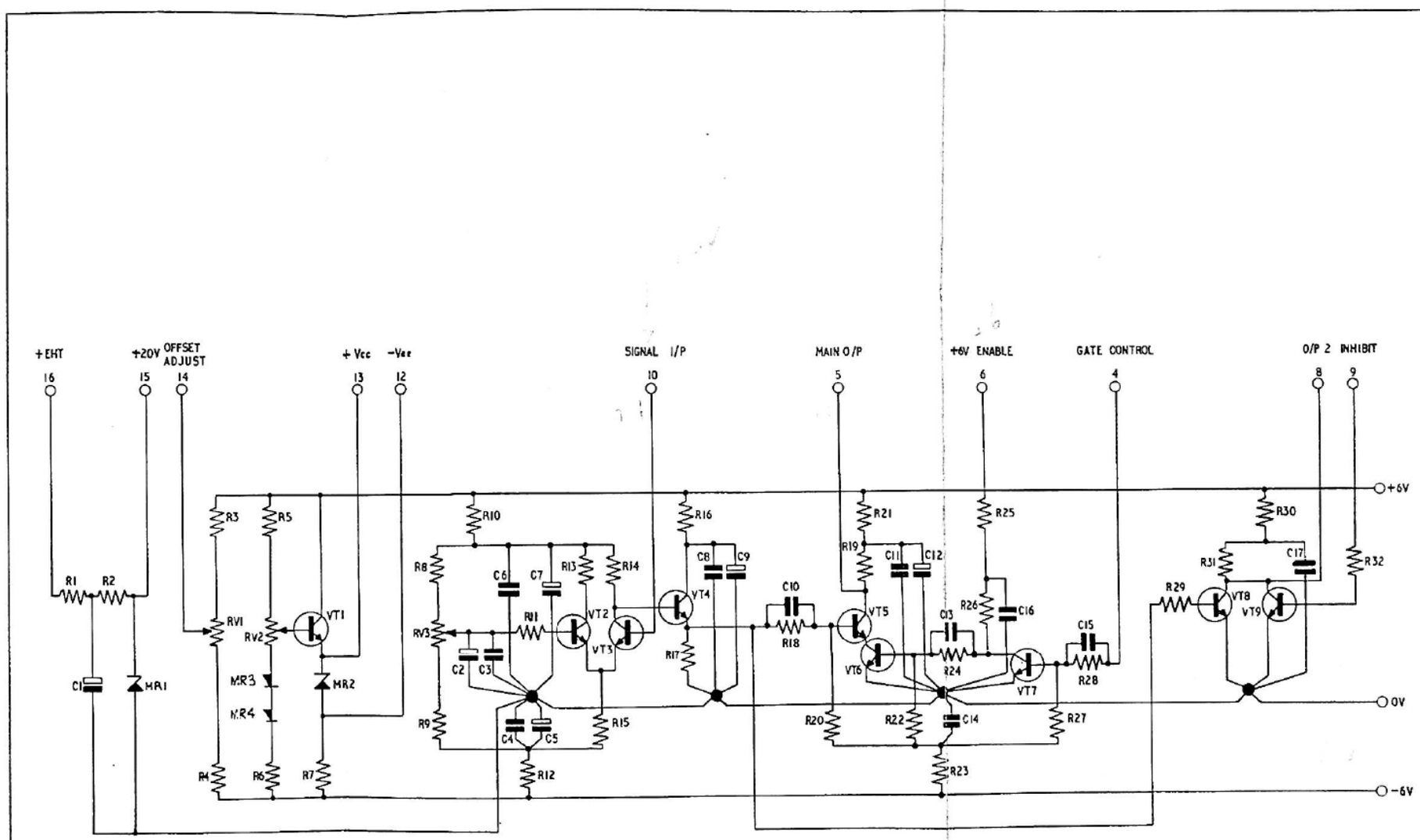
MARCONI INSTRUMENTS LIMITED TF 2414A

Youtube.com/TonyAlbus
73 Tony PE1ONS

POWER SUPPLY

TYPE 66/210

DRG.NO. E66/98 **ISSUE B**

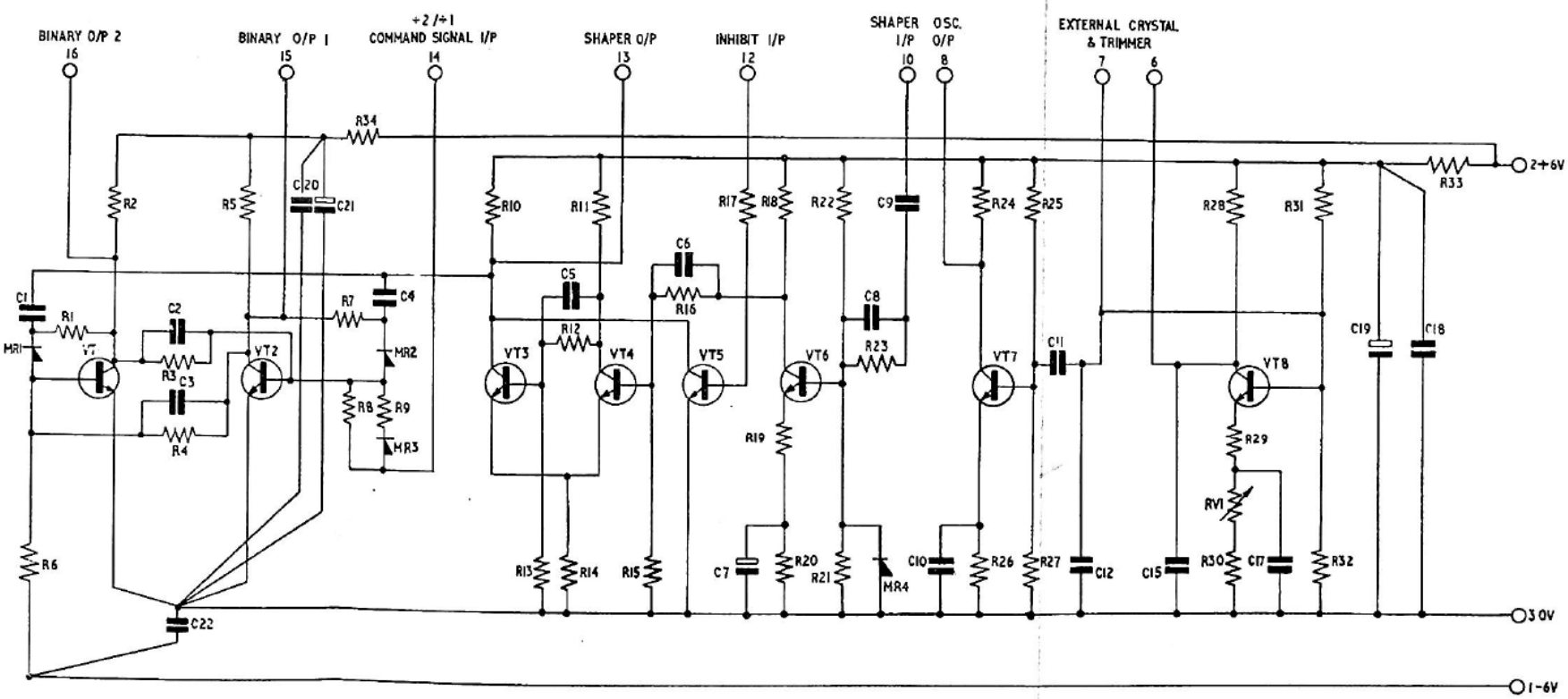


LAST R-32
LAST C-17
LAST MR-4
LAST VT-9
LAST RV-3

MARCONI INSTRUMENTS LIMITED TF 2414A

PULSE SHAPER

TYPE 66/330
DRG. NO. E67/83



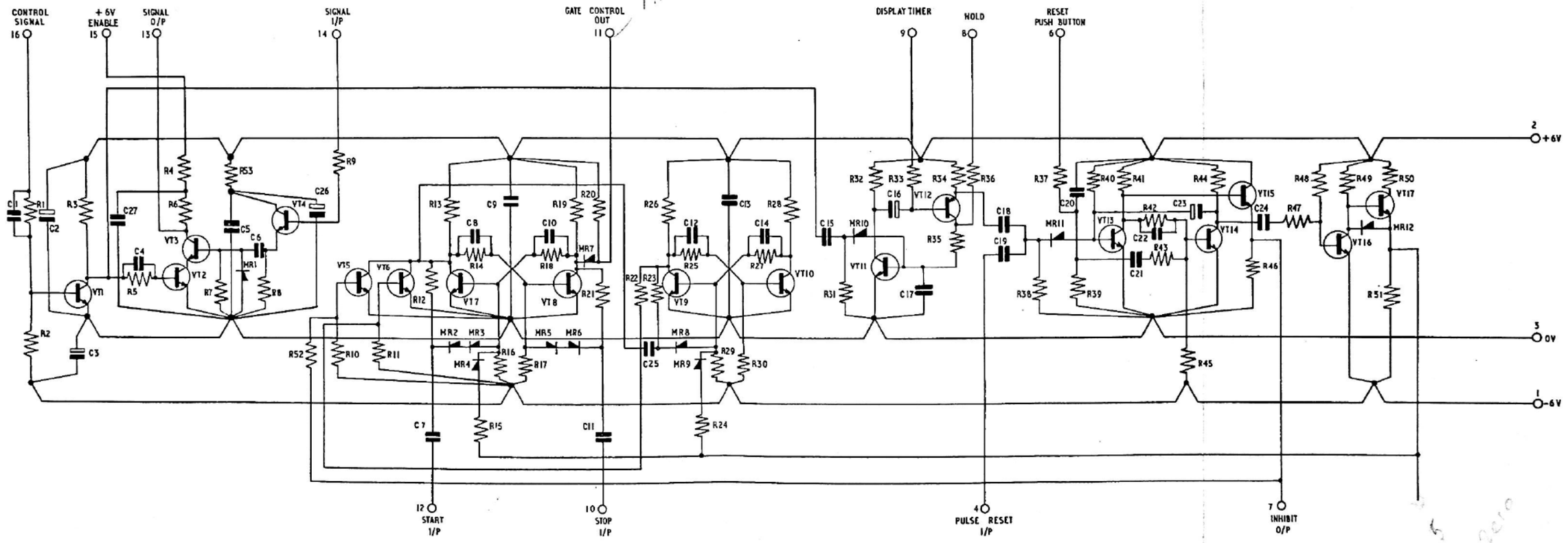
LAST R-34
LAST C-22 C13,14,16, NOT USED.
LAST MR-4
LAST VT-8
LAST RV-1

Youtube.com/TonyAlbus
73 Tony PE1ONS

MARCONI INSTRUMENTS LIMITED TF 2414A

OSCILLATOR

TYPE 66/520
DRG. NO. E67/82

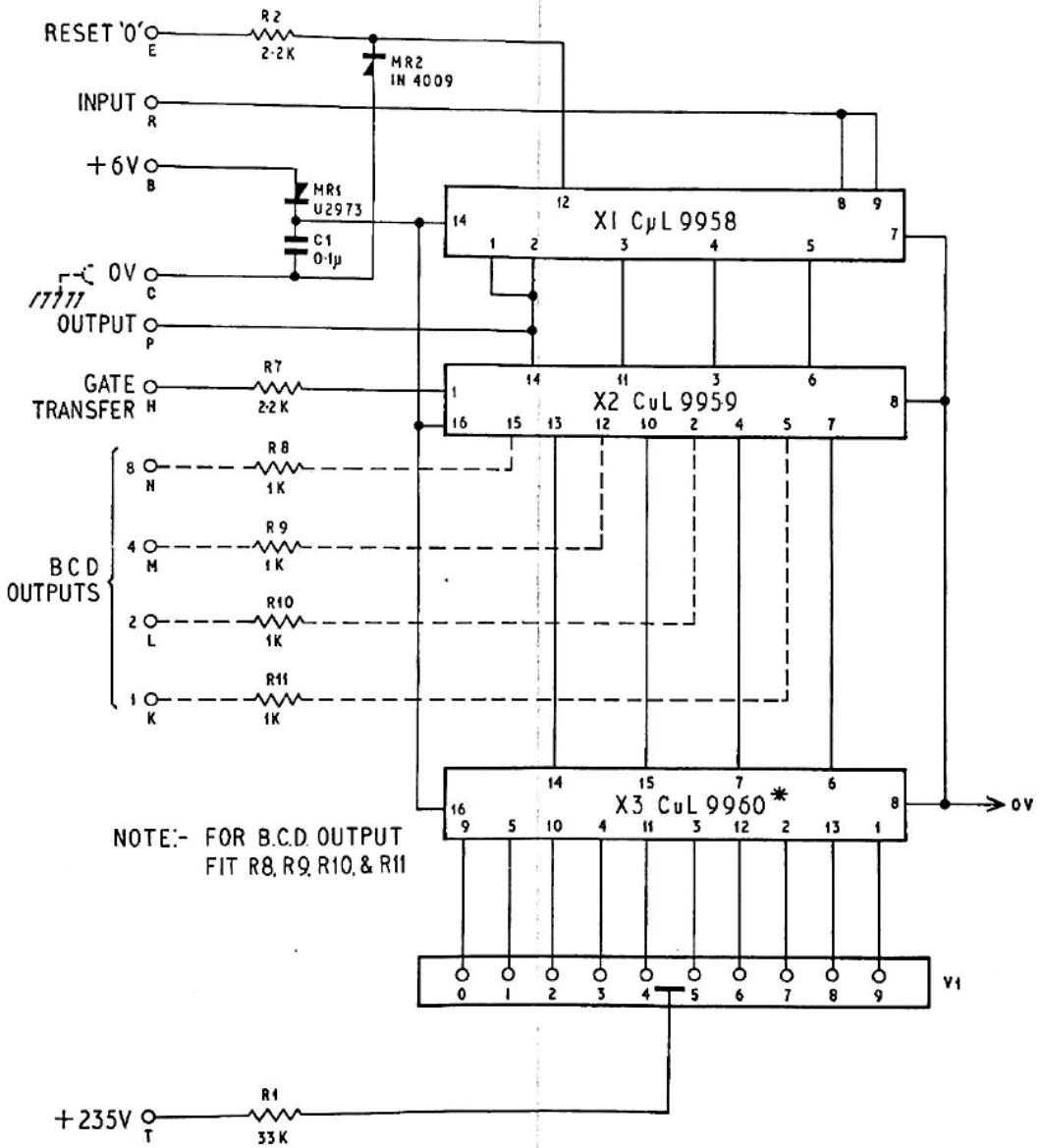


Youtube.com/TonyAlbus
73 Tony PE1ONS

MARCONI INSTRUMENTS LIMITED TF 2414A

GATE CONTROL AND RESET CIRCUIT

TYPE 66/630
DRG. NO. E 67/60

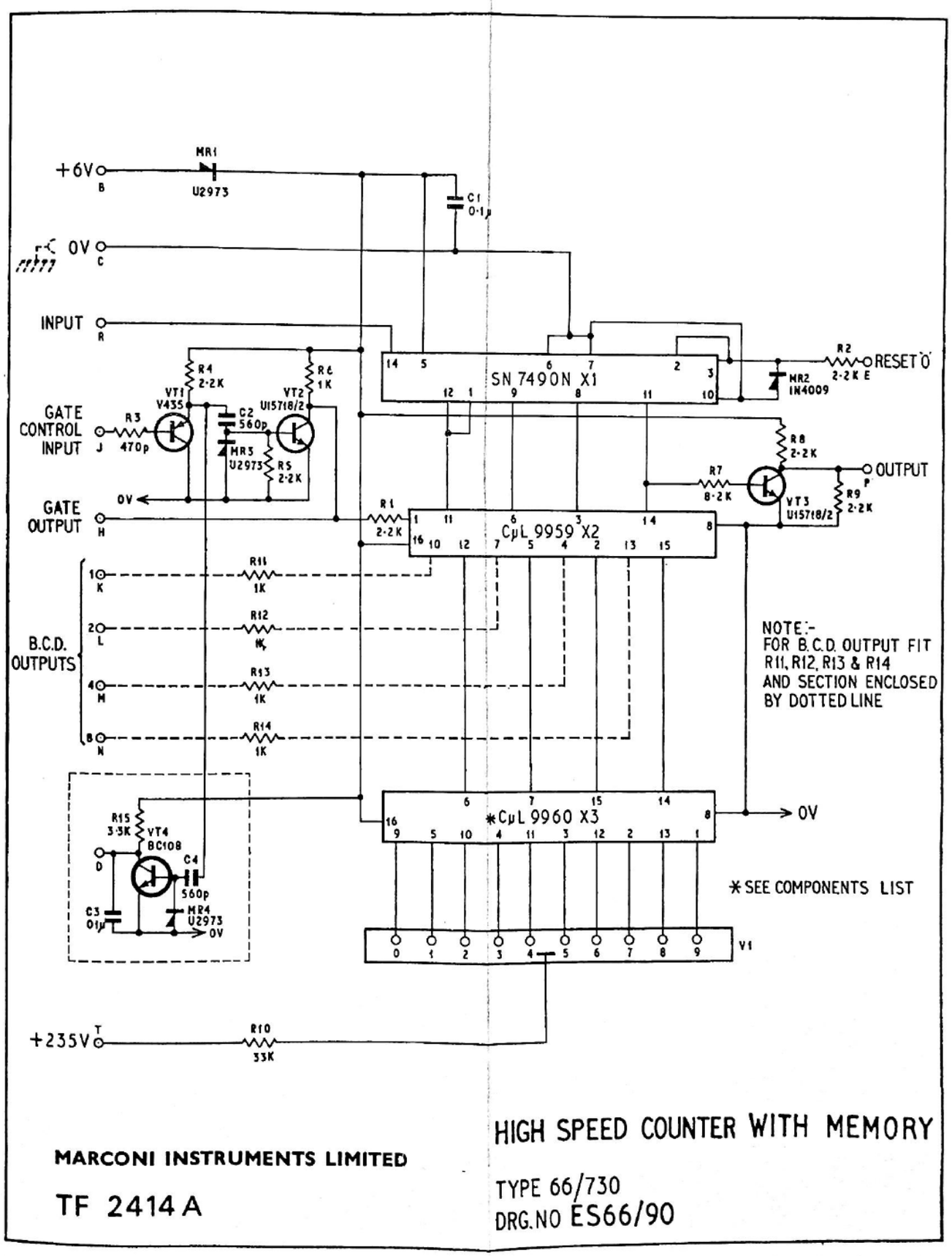


* SEE COMPONENTS LIST

MARCONI INSTRUMENTS LIMITED

TF 2414A

LOW SPEED INTEGRATED COUNTER
WITH MEMORY
TYPE 66/710/M
DRG. NO. ES66/89 ISSUE B

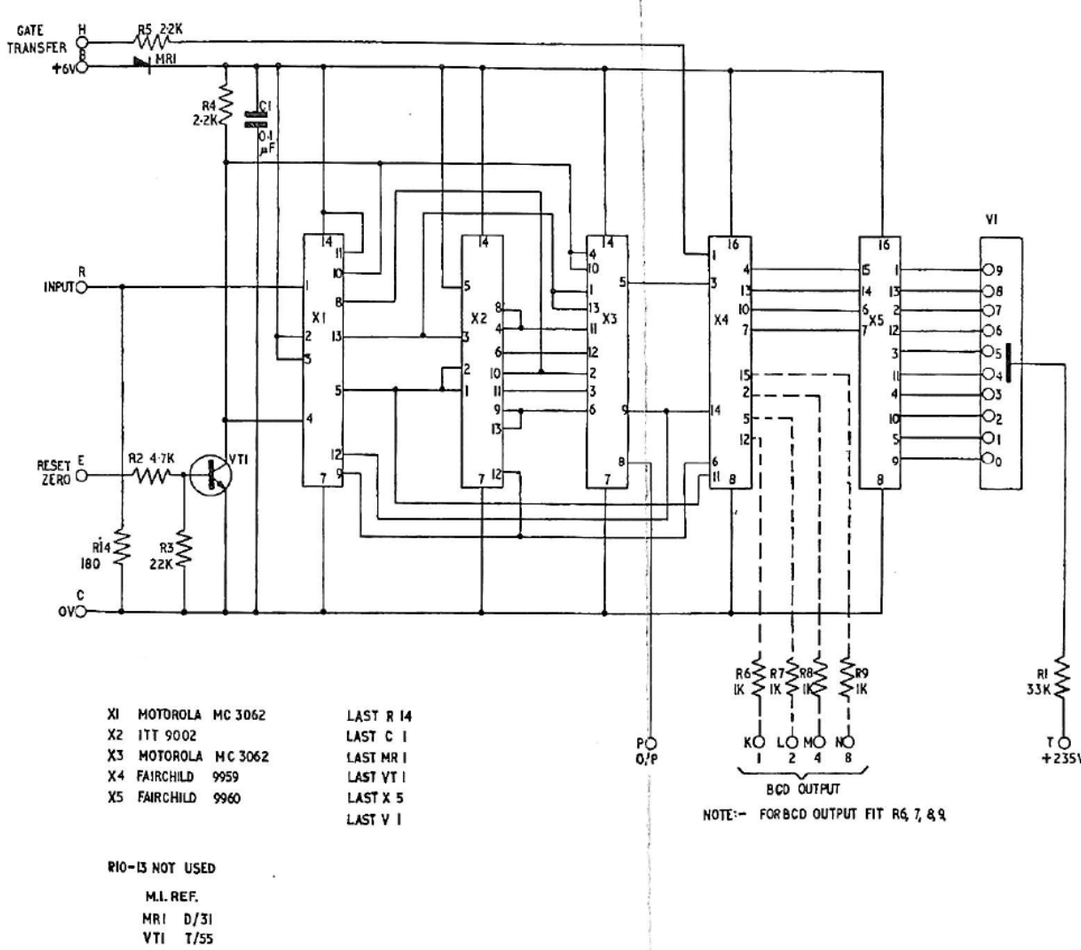


MARCONI INSTRUMENTS LIMITED

TF 2414 A

HIGH SPEED COUNTER WITH MEMORY

TYPE 66/730
DRG.NO ES66/90



X1 MOTOROLA MC 3062
X2 ITT 9002
X3 MOTOROLA MC 3062
X4 FAIRCHILD 9959
X5 FAIRCHILD 9960

LAST R 14
LAST C 1
LAST MR 1
LAST VT 1
LAST X 5
LAST V 1

R10-13 NOT USED

M.I. REF.
MR1 D/31
VT1 T/55

NOTE:- FOR BCD OUTPUT FIT R6, 7, 8, 9

HIGH SPEED INTEGRATED COUNTER WITH MEMORY

TYPE 66/740M
DRG. NO. E67/85

Youtube.com/TonyAlbus
73 Tony PE1ONS

MARCONI INSTRUMENTS LIMITED TF 2414A